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Dynamic Memory Cells Using MoS$_2$ Field-Effect Transistors

Demonstrating Femtoampere Leakage Currents

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ABSTRACT

Two-dimensional semiconductors such as transition metal dichalcogenides (TMDs) are of tremendous interest for scaled logic and memory applications. One of the most promising TMDs for scaled transistors is molybdenum disulfide (MoS$_2$), and several recent reports have shown excellent performance and scalability for MoS$_2$ MOSFETs. An often overlooked feature of MoS$_2$ is that its wide band gap (1.8 eV in monolayer) and high effective masses which should lead to extremely low off-state leakage currents. These features could be extremely important for dynamic memory applications where the refresh rate is the primary factor affecting the power consumption. Theoretical predictions suggest that leakage currents in the $10^{-18}$ to $10^{-15}$ A/µm range could be possible, even in scaled transistor geometries. Here, we demonstrate the operation of one- and two-transistor dynamic memory circuits using MoS$_2$ MOSFETs. We characterize the retention times in these circuits, and show that the two-transistor memory cell reveals MoS$_2$ MOSFETs leakage currents as low as $1.7 \times 10^{-15}$ A/µm, a value that is below the noise floor of conventional dc measurements. These results have important implications for the future use of MoS$_2$ MOSFETs in low-power circuit applications.

Keywords: MoS$_2$, MOSFET, memory, 2D materials, transition metal dichalcogenides
Transition metal dichalcogenides (TMDs) have been of great interest recently for a wide range of electronic and photonic device applications.\(^1\) Several different TMDs have recently been investigated for use in metal-oxide-field effect transistors (MOSFETs),\(^2\)--\(^9\) and various types of circuit demonstrations have been reported aimed at logic,\(^10\)--\(^17\) analog,\(^18\),\(^19\) and memory applications.\(^20\)--\(^25\) While the range of TMDs under investigation in the literature has expanded greatly, molybdenum disulfide (MoS\(_2\)), one of the earliest TMDs investigated for devices,\(^2\) remains one of the most promising candidates for practical applications. In particular, there is one aspect of MoS\(_2\) MOSFETs that has not received significant attention, which is their potential for extremely-low leakage operation. MoS\(_2\) has a band gap, \(E_g\), of \(~1.8\) eV in monolayer\(^26\) and \(~1.3\) eV for multi-layer\(^27\) and effective mass, \(m^*\), \(~0.5m_0\) for electrons and holes,\(^27\) where \(m_0\) is the free electron mass. Silicon has narrower band gap of \(E_g = 1.1\) eV and tunneling-relevant \(m^* \sim 0.2m_0\).\(^28\) For these reasons, combined with its potential for monolayer thickness, short channel effects (SCEs) and gate induced drain leakage (GIDL) are expected to be substantially suppressed in MoS\(_2\) compared to silicon and many of the narrower-gap TMDs, making MoS\(_2\) suitable for extremely-low leakage static and dynamic memories.\(^29\)

In memory applications, particularly dynamic memories, the MOSFET leakage requirements can be quite different from those in logic circuits. In the latter, the most important figure of merit is the subthreshold slope, \(SS\), which ensures the lowest possible off-state current (at zero gate bias) while still maintaining acceptable drive current. Furthermore, for logic devices, there are severe constraints on the supply voltage, \(V_{DD}\), which must be kept as low as possible, since these devices have high activity factor, and the active power consumption goes as \(V_{DD}^2\). However, for memory circuits, the \(V_{DD}\) requirement can be relaxed substantially, since the activity factor is much lower. For instance, it is typical for static random accesses memory (SRAM) circuits to
operate at higher $V_{DD}$ than the accompanying logic in order to allow higher threshold devices and thus lower leakage currents.\textsuperscript{30} Further still, in dynamic memory circuits, negative supply voltages are often utilized for the word line bias, in order to ensure that the access transistor can be operated at a gate voltage that provides the minimum leakage current.\textsuperscript{31-34} Therefore, for many memory applications, it is the minimum current, $I_{\text{MIN}}$, rather than $SS$, that is the most important figure of merit for low-power operation. Furthermore, since DRAM power is dominated by the refresh process, and due to the fact that the refresh rate is proportional to $I_{\text{MIN}}$,\textsuperscript{29} then the total power consumption should also decrease proportional to $I_{\text{MIN}}$, provided that all other memory parameters remain the same. Comparison of the theoretical predictions\textsuperscript{29} for MoS$_2$ with experimental results\textsuperscript{32} for silicon suggest that two orders-of-magnitude reduction in refresh power could be possible at fixed cell size using MoS$_2$.

Ensuring the lowest possible minimum current is particularly important in embedded dynamic random access memories (DRAMs) where the fabrication process must be kept compatible with that of the logic circuitry, thus placing constraints on the size of the storage node capacitor. To address this issue, transistor-only memory cells have been proposed which utilize the gate electrode of a MOSFET itself as the storage capacitor. These types of cells, such as the three transistor (3T) gain cell\textsuperscript{34,35} have the advantage that the read and the write operation are de-coupled, thus allowing non-destructive read and further allowing the transistor’s inherent gain to increase the read current. However, such cells have the disadvantage of a low storage node capacitance and thus higher refresh rates. Therefore, in order for such memories to be viable for practical implementation, orders of magnitude improvements in the leakage current are needed, making MoS$_2$ an ideal candidate for such applications.
In this work, we demonstrate the capability of ultra-low (∼1 fA/µm) leakage currents in MoS₂ through the use of dynamic memory cell circuits. In particular, both one transistor / one capacitor (1T/1C), and two transistor (2T) configurations have been realized, and the retention times are characterized for both systems. Based upon the measured retention times, and the estimated capacitance of the device geometry, our results reveal leakage currents far below the noise floor of conventional dc measurements. Interestingly, the leakage current does not follow the trends expected for contact-limited current injection, but instead has a constant minimum current suggestive of Shockley-Read-Hall (SRH) as the mechanism limiting the leakage current.

RESULTS AND DISCUSSION

The device fabrication began by growing ∼100 nm of SiO₂ on a p-type silicon substrate. Alignment marks were then patterned using electron beam lithography (EBL) and Ti/Au metal was used to form alignment marks for subsequent process steps. Next, a local back gate was patterned using EBL and a combination of dry and wet etching was used to etch about 40 nm of SiO₂, followed by deposition and lift off of Ti (10 nm) / Pd (30 nm) using electron beam evaporation. To form the gate dielectric, 20-nm of HfO₂ was deposited at 300 °C using atomic layer deposition (ALD). In order to enable electrical connection between the two transistors, vertical interconnect openings needed to be formed. In order to realize these, an additional Al₂O₃ layer was deposited by ALD and openings were patterned in PMMA using EBL. The Al₂O₃ was then etched over the extrinsic portion of the gate electrode using a wet etch and then reactive ion etching was used to etch the HfO₂. After this etch, the PMMA was removed and the Al₂O₃ hard mask was stripped using a wet etch. Mechanical exfoliation of multi-layer MoS₂ was then performed to position separate MoS₂ flakes over the buried gate electrodes. Finally, Ti (10 nm) / Au (100 nm) was deposited to form source and drain contacts as well as to form interconnect
metallization between the two transistors. All devices had a source-to-drain contact separation of 0.5 µm. The MoS$_2$ thickness varied slightly from device to device, but was approximately 5-7 nm for all devices. While monolayer MoS$_2$ would be preferred for DRAMs due to its larger energy gap, substantial leakage benefit is still expected due to the larger energy gap of few-layer MoS$_2$ and higher effective mass compared to silicon.$^{27}$ Stand-alone MoS$_2$ n-MOSFETs, and both 1T/1C and 2T memory circuits were fabricated. Fig. 1a shows a schematic diagram of our locally-backgated MoS$_2$ MOSFET structure and an optical micrograph of a stand-alone device is shown in Fig. 1b.

Initial electrical characterization was performed on single devices fabricated on the same wafer as the circuits that will be described later in this manuscript. The measurements were performed using an Agilent B1500A semiconductor parameter analyzer. A typical drain current, $I_D$, vs. gate voltage, $V_G$, characteristic for a MoS$_2$ n-MOSFET is shown in Fig. 1c. The results show that the locally backgated MOSFETs have excellent turn-off characteristics with linear subthreshold slope in both the linear and saturation regimes. No measurable gate leakage current could be detected for all bias voltages utilized in these studies. The linear-regime subthreshold slope vs. current curves for several isolated devices are plotted in Fig. 1d, and this plot shows that the minimum $SS$ value ranged between ~ 65-80 mV/decade, corresponding to an interface trap density, $D_{it}$, in the range of 0.4-1.5 $\times$ 10$^{12}$ cm$^{-2}$/eV. For these measurements no evidence of GIDL was observed and so it is clear that $I_{MIN}$ is below the noise floor, and therefore, an accurate value of $I_{MIN}$ could not be determined using DC measurements.

Initial retention time characterization of dynamic memory cells was performed using a 1T/1C circuit configuration. A diagram of the 1T/1C cell is shown in Fig. 2a, along with a micrograph of the circuit that was characterized in Fig. 2b. In this circuit, a metal-insulator-metal (MIM)
capacitor was formed by overlapping the contact metallization with gate-level metallization and integrating with a MoS$_2$ n-MOSFET. The capacitor had an area of 50 x 50 µm$^2$, and thus had a total capacitance of 18 pF, based upon the HfO$_2$ thickness of 20 nm and a dielectric constant of 16.6 for HfO$_2$ (as determined from separate measurements on stand-alone metal-insulator-metal capacitors).

The measurement of the 1T/1C cell was performed using an AC measurement technique similar to that used in conventional DRAM arrays. In these measurements, a multi-channel pulse generator was utilized to enable data writing and reading. As depicted in Fig. 2c, during the write operation, the drain voltage of the transistor acts as the write bit line (WBL) and is raised from 0 to 1 V. This action triggers the write word line (WWL), which is the gate electrode of the transistor, to be raised from $V_G = -1.5$ V to $+1.0$ V, where $-1.5$ V is the bias of the transistor in the retention (hold) mode of the memory cell. The pulses on WBL and WWL are synchronized such that the bit line voltage is raised 10 µs earlier and is lowered 10 µs later than the word line voltage. For the duration of the write operation, the transistor is in the on state and thus charges the capacitor to the potential of the bit-line voltage (either 0 or 1 V). The duration of the WWL pulse was chosen so as to ensure that the capacitor is fully charged. To read the data, the potential on the storage-node capacitor is compared with one half of the bit line voltage (in this case, 0.5 V) and the stored information is determined by the sign of the charge flowing out of or into the storage node.

This pulse sequence can be seen in the oscilloscope traces shown in Figs. 2d and 2e. For the measurements shown in Fig. 2d, a short hold time, $t_{\text{HOLD}}$, of 50 µs was investigated. For this sequence, a “1” was written during the write cycle and then the value read out during the read cycle. Because of the short time interval, the charge is retained on the capacitor, and therefore,
when 0.5 V is applied to the bit line, the capacitor discharges leading to a negative current flow “spike”. Here, the current is read out as the voltage across a 20 kΩ resistor placed between the storage capacitor and ground. The situation for a long hold time ($t_{\text{HOLD}} \sim 1 \text{ s}$) is shown in Fig. 2e. In this case, the subthreshold leakage causes the charge to slowly “bleed” off of the storage node, leading to a loss of the stored data. Therefore, the voltage across the capacitor drops below the applied voltage of 0.5 V on the bit line during the read operation. This means the current flow during read will not change sign, but instead, will be the same sign as the original write “1”. In this way the retention time of the 1T/1C cell can be determined.

To characterize the retention time, $\tau_{\text{ret}}$, of the 1T/1C cell, automated measurements were performed where write and read pulses were applied in succession with varying the hold time ($i.e.$, the interval between write and read pulses). The value of $t_{\text{HOLD}}$ was varied from 10 µs to 1 s on a log scale with 20 points per decade. Here, the read charge, $Q_{\text{READ}}$, is calculated as the time integral of the current measured from the start of the read pulse to the start of the next write pulse. For a hold voltage (the voltage applied to WWL in Fig. 2a) of $V_{\text{HOLD}} = -1.5 \text{ V}$, we obtain a value of $\tau_{\text{ret}} = 251 \text{ ms}$, where the retention time is defined as the interval time at which $Q_{\text{READ}} = 0$. It is important to note that even at $\tau_{\text{ret}} = 251 \text{ ms}$, some charge is still stored on the capacitor node. Fig. 2f shows $Q_{\text{READ}}$ vs plotted vs. $t_{\text{HOLD}}$ for the 1T/1C cell for different values of $V_{\text{HOLD}}$. It can be seen that the retention time decreases with increasing (less negative) values of $V_{\text{HOLD}}$. This is expected as the device is not fully turned off at these voltages and thus the leakage of the transistor dramatically increases. The plot in Fig. 2f does show a small “plateau” in the $Q_{\text{READ}}$ vs. $t_{\text{HOLD}}$ characteristic, which is indicative of partial discharge of the capacitive node after the write sequence, with a time constant on the order of $\sim 1 \text{ ms}$. The precise nature of this discharge is unclear at this point, but does not have a large effect on the extracted value of $\tau_{\text{ret}}$. The maximum
value of $Q_{\text{READ}}$ also shows a small decrease for $V_{\text{HOLD}} = -1.3$ V and $-1.5$ V, which we believe is associated with a small decrease in the on-state current of transistor T1 after repeated measurement cycling. This could lower the apparent stored charge due to the fact that only a limited time window (200 µsec) was used to perform the read operation. Despite these minor anomalies, the 1T/1C leakage current, $I_{\text{LEAK}}$, can be estimated directly from the retention time using the formula $I_{\text{LEAK}} = C_1 V_1 / \tau_{\text{RC}}$, where $C_1 = 18$ pF is the storage node capacitance, $V_1 = 1.0$ V is the write voltage, and $\tau_{\text{RC}} = \tau_{\text{ret}} / \ln(2)$. Using the value for the capacitance determined previously, we obtain values for $I_{\text{LEAK}}$ vs. $V_G$, and the results are shown in Fig. 2g, where $I_{\text{LEAK}}$ is observed to decrease down to 17 pA/µm at $V_{\text{HOLD}} = -1.5$ V. While the corresponding DC leakage currents for this particular device cannot be extracted directly, the results are roughly consistent with the subthreshold characteristics from the stand-alone device shown in Fig. 1c, though we have found that our MoS$_2$ MOSFETs can have some deviations in their threshold voltages from device to device. Unfortunately, using the 1T/1C geometry, longer retention times could not be measured using our pulsed technique due to the fact that the oscilloscope cannot trigger at frequencies less than 1 Hz. In the next section, we describe how the use of a 2T circuit can overcome this limitation and allow detection of orders-of-magnitude lower leakage currents.

A circuit diagram of the 2T MoS$_2$ memory configuration is shown in Fig. 3a. This cell consists of two transistors, a write transistor (T1), and a storage/read transistor (T2). The operation of the cell is shown in Fig. 3b: when transistor T1 is turned on, data is written onto the gate of transistor T2, where this gate performs the same function as the storage capacitor in a 1T/1C cell. The charge stored on the gate of transistor T2 changes its conductance, and so the memory state can be read out simply by measuring the current through T2. This type of cell is typically referred to as a “gain cell” since the charge stored on the gate electrode is amplified by
the transistor. The gain cell also has the advantage that it separates the read and write functions allowing non-destructive readout. However, since the overall capacitance of the storage node is lower than that of the 1T/1C cell, if the leakage current is fixed, then the retention time is also lower. While, in silicon technology, this is a disadvantage since it leads to shorter retention times, for MoS$_2$ MOSFETs, long retention times can still be achieved due to the lower “leakage floor.” In addition, for our measurements, the 2T geometry enables measurement of these low leakage currents more easily, due to the low value of the stored charge. An optical micrograph of the sample used for these measurements is shown in Fig. 3c, where two separate flakes were used for transistors T1 and T2. Atomic force microscopy (AFM) was used to determine the MoS$_2$ thickness and both flakes had similar thickness. The MoS$_2$ flake for T1 was ~ 7 nm thick (Fig. 3d), while T2 had a flake thickness of ~ 6 nm (Fig. 3e).

An estimate of the retention time of the gain cell can be made by writing data onto the gate of transistor T2 and observing the discharge of the current over time. This discharge is a direct indicator of the leakage current in transistor T1. We performed two sets of measurements in order to determine the retention characteristics and extract the value of $I_{\text{LEAK}}$ in the 2T geometry. As depicted in Fig. 3b, in our initial set of measurements, synchronized pulses were applied to the bit line and word line, and then the resulting change in current through transistor T2 was observed by measurement the voltage across a 20 kΩ resistor (R2 in Fig. 3a) which was connected in series with T2. Additional details of the measurement setup and pulse sequence are described in the Methods section.

The retention time measurement results are shown in Fig. 4a, where the current through T2 is plotted vs. time on a log scale for $V_{\text{HOLD}} = -1.0$ V to $-1.6$ V. For these measurements, we considered the 2T retention time, $\tau_{\text{ret}}$, to be the time required for the current to drop to 50% of its
original value at the end of the write pulse. This retention time changes exponentially based on the value of $V_{\text{HOLD}}$ applied to the gate of the write transistor (T1) as shown in Fig. 4b. As expected, as $V_{\text{HOLD}}$ is made more negative, the value of $\tau_{\text{ret}}$ increases as T1 is biased more into the off-state. In order to quantify this effect, we once again extracted the effective leakage current through T1 using the formula: $I_{\text{LEAK}} = C_2 V_2 / \tau_{\text{RC}}$, where $C_2$ is the storage node capacitance, $V_2 = 1.0$ V is the write voltage, and $\tau_{\text{RC}} = \tau_{\text{ret}} / \ln(2)$. Here, $C_2$ is much lower than the corresponding capacitance for the 1T/1C cell and has an estimated value of $C_2 = 0.051$ pF. Using this technique, $I_{\text{LEAK}}$ vs. $V_{\text{HOLD}}$ can be determined and these results are shown in Fig. 4c. Due to the much lower storage node capacitance used in this circuit, much lower values of $I_{\text{LEAK}}$ can be extracted compared to the 1T/1C circuits. Here, we find leakage currents as low as a few fA/µm.

Even with the improved current resolution of the 2T geometry, leakage currents at lower values of $V_{\text{HOLD}}$ could not be probed due to the limitations of the synchronous measurement technique. Therefore, in order to determine the ultimate retention time, and extract the equivalent leakage current, a quasi-DC method of measuring the 2T memory cell geometry was utilized which allowed retention times $> 1$ sec to be characterized. In this methodology, the retention time of the 2T cell was made by writing data into the storage transistor and simply observing the discharge of the current over time using a B1500A semiconductor parameter analyzer. Once again, details of the measurement sequence are provided in the Methods section. The results for a series of measurements of the current through transistor T2 vs. time with different values of $V_{\text{HOLD}}$ are shown in Fig. 5a. Here, it is clear that retention times longer than 1 second can be obtained, and we once again defined the retention time as the time required for the current to drop by 50% of its original value at the end of the write pulse. Using this criterion, the retention time was found to be as high as 1.3 sec, but did not change significantly between $V_{\text{HOLD}} = -1.8$ V
and −2.5 V. The extracted leakage current vs. $V_{\text{HOLD}}$, using the same methodology as described previously, is shown in Fig. 5b, where values of $V_{\text{HOLD}}$ from −1.3 V to −2.5 V were characterized. The leakage current does not continue to decrease for $V_{\text{HOLD}} < −1.8$ V, and levels off to a constant value, where the average value of the leakage current between $V_{\text{HOLD}} = −1.8$ V and −2.4 V is $1.70 \pm 0.22$ fA/µm. It is important to note the results in Fig. 5a show that the read current initially drops more steeply for more negative values of $V_{\text{HOLD}}$ before leveling out, and this behavior will be discussed in greater detail below.

To understand the expected leakage limitations in MoS$_2$ MOSFETs, a simple one-dimensional (1D) current model has been employed. The model is developed using a previously-developed model for black phosphorus MOSFETs$^{36}$ which was modified to accommodate few-layer MoS$_2$ as the channel material. As shown in Fig. 5c, the model contains three major leakage current components: 1) thermionic current, 2) gate induced drain leakage (GIDL) which is simply band-to-band tunneling from the channel to the drain and 3) SRH generation. For the thermionic and GIDL currents, a transmission-based formalism was utilized for the current.$^{36}$

Here, the effective masses of electrons and holes were taken to be $0.53m_0$ and $0.43m_0$, respectively.$^{27}$ The band gap of few-layer MoS$_2$ was further assumed to be 1.3 eV.$^{27}$ Finally, an interface trap density of $D_{it} = 2.1 \times 10^{12}$ cm$^{-2}$/eV was fitted to the experimental data, which is close the value extracted from the stand-alone devices in shown in Fig. 1. The modeling results are shown in Fig. 5d for both $V_{DS} =$ +0.5 and +1.0 V, where the minimum current reaches below 1 fA/µm at $V_G =$ −1.5 V. However, as $V_G$ is further decreased to −2.5 V, the modeled current increases to above 10 pA/µm at $V_{DS} =$ +1.0 V, but remains below 1 fA/µm at $V_{DS} =$ +0.5 V. At first, this would seem inconsistent with the experimental results. However, in our memory measurement scheme, as the storage node discharges, the bias across transistor T1 decreases,
which in turn, decreases the leakage current. This is consistent with our observation above regarding the initial steep drop in the read current at the more negative values of \( V_{\text{HOLD}} \). To estimate the leakage current at higher bias based upon this initial current drop, in Fig. 5d, we have also extracted the equivalent leakage current using the 20% current reduction point. This data is shown by the red triangles in Fig. 5d, and indeed shows that the leakage current is higher during the initial discharge stage due to the higher bias voltage across T1. However, the simulations show that once the node voltage reaches +0.5 V, the leakage current should drop well below 0.1 fA/\( \mu \)m, while the experimental points determined using the 50% current reduction criterion remain \( \sim 1 \) fA/\( \mu \)m and are largely bias independent. From these results, we conclude that, after a small partial discharge due to GIDL, the leakage and thus the retention time is limited by SRH generation, shown by the green line in Fig. 5d. While a model for the SRH generation current is difficult to formulate, due to uncertainties in the transport and field distribution beneath the contacts, it is nevertheless reasonable to expect this current to be relatively independent of \( V_G \) and \( V_{DS} \).

CONCLUSION

In conclusion, the operation of MoS\(_2\)-based dynamic memory cells is demonstrated. Both 1T/1C and 2T gain cell memories are demonstrated and retention times up to 0.25 sec and 1.3 sec are achieved for the 1T/1C and 2T cells, respectively. Perhaps more importantly, characterization of these circuits allows exploration of current levels difficult to achieve with conventional methods. In particular, we have demonstrated the measurement of leakage currents on the order of 1-2 fA/\( \mu \)m with the prospect to explore lower currents in future experiments. Furthermore, we show that the minimum leakage current is not dominated by tunneling or thermionic currents, but is likely due to SRH generation, possibly arising from defects in the
MoS$_2$ or the MoS$_2$/dielectric interfaces. These results could be important for the future understanding of MoS$_2$ MOSFETs for low standby power applications.

**METHODS**

*Device and integrated circuit fabrication.* The fabrication of the inverter circuit started with dry thermal oxidation of a 100-nm-thick SiO$_2$ layer on a Si substrate. Alignment marks were first patterned on the substrate by spinning polymethylmethacrylate (PMMA) and then patterning using a Vistec EBPG 5000+ electron-beam lithography (EBL) system. After development in 1:3 MIBK:IPA and rinsing in isopropanol (IPA), Ti / Au (10 nm / 100 nm) was deposited using electron-beam evaporation followed by a solvent lift-off in acetone followed by an IPA rinse. Next, the local back gate contacts were patterned. Once again, PMMA was spin-coated on the wafer and EBL was used to pattern 3-µm wide, 80-µm long stripes connected to enlarged pad regions for wafer probing. After development in 1:3 MIBK:IPA + an IPA rinse, the sample went through a 5 s O$_2$ plasma clean to remove PMMA residues then CHF$_3$/CF$_4$/Ar reactive ion etching was performed with to create about 40-nm deep recess in the SiO$_2$ layer. The sample was then etched in buffered oxide etch (BOE) for 12 seconds to create a roughly 40-nm recess in the SiO$_2$. After the recess etch, Ti / Pd (10 nm / 30 nm) was evaporated using electron-beam evaporation and lifted off in acetone and rinsed in IPA. After the gate lift off, 20 nm of HfO$_2$ was deposited using atomic layer deposition (ALD) using tetrakis(dimethylamido) hafnium(IV) and water vapor as the precursors. To form the vertical interconnect openings over the gate electrode, a hard mask of Al$_2$O$_3$ was deposited using ALD. The openings were patterned in PMMA using EBL and developed as above. Next, the Al$_2$O$_3$ was etched using BOE for 120 seconds. This was followed by reactive ion etching of the HfO$_2$ in a CF$_4$ / Ar plasma. PMMA was then stripped in acetone followed by an IPA rinse, and the remainder of the Al$_2$O$_3$ was removed using BOE.
MoS$_2$ flakes, mechanically exfoliated from bulk crystals (purchased from SPI), were aligned and transferred to the local back gate regions using a polydimethylsiloxane (PDMS) stamp attached to a glass slide using a homemade optical alignment station. A solvent clean was performed to remove PDMS residue and then PMMA was spin-coated on the samples. Finally, for source and drain contacts, EBL was used to pattern the features using the same process as above and after development, Ti / Au (10 nm / 100 nm) metallization was evaporated and lifted-off in acetone/IPA to complete the circuit fabrication. After the final lift off, the sample was loaded into the vacuum chamber of the cryogenic probe station for testing. No surface passivation was utilized. Atomic force microscopy (AFM) was utilized to determine the thickness of the flakes on the MOSFETs in the 2T circuit after all measurements had been completed.

**Device and memory cell characterization.** All of the device and memory cell characterization was performed under vacuum conditions ($\sim 10^{-5}$ Torr) at room temperature using a Lakeshore CPX-VF cryogenic probe station with triaxial probe feedthrough connections. For the DC quasi-DC current 2T measurements, an Agilent B1500A semiconductor device parameter analyzer was utilized. For the pulsed AC measurements, a two-channel Keysight 33522B function generator was utilized, where two channels were used to supply the square wave input waveform for the word and bit lines. Both the input and output waveform data were monitored with a two-channel Keysight 3014C digital oscilloscope. Both function generator and oscilloscope were controlled through a GPIB interface. Matlab and python code were utilized to generate appropriate waveforms, and command / control the measurements. All the testing channels and the circuit shared a common ground terminal.
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AUTHOR CONTRIBUTIONS

CUK, WX, CHK, and SJK designed and directed this study and analyzed the results. CUK, YS and MCR performed device fabrication. CUK, YS, and SJK performed process development. CUK, WX, MCR, CHK and SJK performed device characterization. CUK and SJK wrote the manuscript.

ADDITIONAL INFORMATION

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COMPETING FINANCIAL INTERESTS

The authors declare no competing financial interests.
REFERENCES


Figure 1. Characteristics of locally-backgated few-layer MoS$_2$ MOSFET utilized in this work. (a) Illustration of a typical MoS$_2$ MOSFET showing source, drain and gate electrodes. (b) Optical image of the MoS$_2$ MOSFET showing source drain and gate electrode configuration. (c) Drain current vs. gate voltage for a typical MoS$_2$ MOSFET at $V_{DS} = +0.1$ V and +1.0 V. The subthreshold slope at $V_{DS} = +0.1$ V was 77 mV/decade and showed virtually change at higher $V_{DS}$. (d) Subthreshold slope vs. drain current for several MoS$_2$ MOSFETs. The devices had minimum subthreshold slopes between 65-80 mV/decade, corresponding to interface trap density values of $0.4$-$1.5 \times 10^{12}$ cm$^{-2}$/eV.
Figure 2. One transistor / one capacitor (1T/1C) memory cell description and measurement results. (a) Circuit schematic of 1T/1C circuit. (b) Optical image of 1T/1C cell using MoS$_2$ MOSFET (T1) and metal-insulator-metal (MIM) capacitor (C1). The resistor, R1, which is connected externally, is not part of the memory cell and is only used to determine the current during read and write operations. (c) Illustration of 1T/1C memory cell operation showing input and output signals at the write and read lines. (d) Example of memory operation using a hold time of 50 \( \mu \text{s} \). The bit line pulse is red, the world line pulse is green and the output current (extracted from the voltage across R1) is shown in black. The sign of the current is opposite during the read pulse compared to the write pulse, indicating that the charge has been retained. (e) Same measurement sequence as in (d), except for a hold time of 1 s. Here, the readout current has the same sign as the current during the write pulse, indicating charge has been lost. (f) Calculated retained charge as function of hold time for \( V_{\text{HOLD}} \) values of –1.5 V (black), –1.3 V (red), –1.1 V (green), –0.9 V (blue), and –0.7 V (orange). (g) Estimated leakage current, \( I_{\text{LEAK}} \), as a function of \( V_{\text{HOLD}} \) extracted from the data in (f). It can be observed that the leakage estimate follows the general shape as the transfer characteristic shown in Fig. 1, with a moderate shift in threshold voltage.
Figure 3. Two transistor (2T) memory cell description. (a) Circuit schematic of 2T memory circuit. The resistor, R2, which is connected externally, is not part of the memory cell and is only used to determine the current during read and write operations for the data shown in Fig. 4. For the data shown in Fig. 5a, R2 was not utilized. (b) Optical image of 2T cell using showing both MoS$_2$ MOSFETs. (c) Illustration of 2T memory cell operation showing input and output signals at the write and read lines. (d) AFM line scan of MoS$_2$ used for transistor T1. (e) AFM line scan of MoS$_2$ used in transistor, T2.
Figure 4. Two transistor (2T) memory cell measurement results. (a) Output current for 2T memory cell with $V_{\text{HOLD}}$ varying from $-1.0$ V to $-1.6$ V in steps of $-0.02$ V. The color sequence is black ($-1.0$ V), red ($-1.02$ V), magenta ($-1.04$ V), blue ($-1.06$ V), and green ($-1.08$ V), and then repeated for each 0.1 V range. (b) Extracted retention time plotted vs. hold voltage, $V_{\text{HOLD}}$. (c) Estimated leakage current as a function of $V_{\text{HOLD}}$. It can be observed that the leakage follow the typical shape of the stand-alone transfer characteristic.
Figure 5. Two transistor (2T) memory cell quasi-DC measurement results and analysis. (a) Output current with $V_{\text{HOLD}}$ varying from $-1.3$ V to $-2.5$ V in steps of $-0.1$ V. It can be observed that after an initial dramatic increase in retention time, the retention time does not change drastically. (b) Estimated leakage current as a function of $V_{\text{HOLD}}$ with 50% discharge as a criterion for retention time. Here, blue dots represent leakage currents extracted from the pulsed readout measurements in Fig. 4, while the red dots represent DC current measurements using the Agilent B1500A. (c) Diagram showing leakage mechanisms for a Schottky source/drain MoS$_2$ MOSFET including thermionic current, Shockley-Read-Hall (SRH) and gate-induced drain leakage (GIDL). (d) Comparison of experimental (symbols) and modeled current components (lines). The equivalent leakage current was extracted based upon time constants extracted from both the 50% (open circles) and 20% (solid triangles) current reduction points in (a). The thermionic and GIDL components are shown with blue dashed lines at $V_{\text{DS}} = +0.5$ V and $V_{\text{DS}} = +1.0$ V, while a constant, bias-independent, SRH component is shown by the solid green line.
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