An Analytical Model for Negative Bias Temperature Instability

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***Abstract*— Negative Bias Temperature Instability (NBTI) in PMOS transistors has become a significant reliability concern in present day digital circuit design. With continued scaling, the effect of NBTI has rapidly grown in prominence, forcing designers to resort to a pessimistic design style using guard-banding. Since NBTI is strongly dependent on the time for which the PMOS device is stressed, different gates in a combinational circuit experience varying extents of delay degradation. This has necessitated a mechanism of quantizing the gate-delay degradation, to pave the way for improved design strategies. Our work addresses this issue by providing a procedure for determining the amount of delay degradation of a circuit due to NBTI. An analytical model for NBTI is derived using the framework of the Reaction-Diffusion model, and a mathematical proof for the widely observed phenomenon of frequency independence is provided. Simulations on ISCAS benchmarks under a 70nm technology show that NBTI causes a delay degradation of about 8% in combinational logic based circuits after 10 years ($\approx 3 \times 10^8$s).**

I. Introduction

When a PMOS transistor is biased in inversion, the dissociation of $Si-H$ bonds along the silicon-oxide interface, causes the generation of interface traps. The rate of generation of these traps is accelerated by temperature, and the time of applied stress. These traps cause an increase in the threshold voltage ($|V_{th}|$) of the PMOS transistors. An increase in V_{th} causes the circuit delay to degrade, and when this degradation exceeds a certain magnitude, the circuit may fail to meet its timing specifications. This effect, known as Negative Bias Temperature Instability (NBTI), has become a reliability issue in high-performance digital IC design, especially in sub-130nm technologies [1]–[7].

Experiments have shown that the application of a negative bias ($V_{gs} = -V_{dd}$) on a PMOS transistor leads to the generation of interface traps, while removal of the bias ($V_{gs} = 0$) causes a reduction in the number of interface traps due to annealing [1]–[4], [7], [8]. Thus, the impact of NBTI on the PMOS transistor depends on the amount of time the device has been stressed, and relaxed. Since a digital circuit consists of millions of nodes with differing signal probabilities and activity factors, asymmetric levels of degradation are experienced by various timing paths. Logic blocks in a circuit are presently designed by assuming a certain safety margin in the timing specifications to account for NBTI-induced performance degradation. Due to the lack of efficient techniques to accurately estimate the temporal degradation of various paths in digital circuits, the safety margin is usually added as a fudge factor, whose magnitude is determined by experiments on test-chips and I_{dsat} degradation measurements. However, such schemes may tend to be excessively pessimistic and lack accuracy.

In this paper, we develop the first analytical model for simulating NBTI over multiple cycles of stress and relaxation. Our work uses the classical Reaction-Diffusion (R-D) model to analytically capture the physical effects of both these stress and relaxation phases of NBTI. Note that although the R-D model has been used in [3]–[5] to physically explain the NBTI action, all of these models have been restricted to a single stress cycle, or a single stress cycle followed by a single relaxation cycle. The subsequent phases of stress and relaxation are handled in [3] by numerically solving the R-D model equations. In contrast, our work builds a comprehensive analytical model, over *multiple* stress/relaxation phases, and also leads to a concrete proof of the frequency-independence property of NBTI.

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Further, our model captures the recently observed shift in time dependence of NBTI from $t^{\frac{1}{4}}$ to $t^{\frac{1}{6}}$ (owing to the argument that the diffusing species is neutral H_2 molecule as opposed to the previously assumed neutral H atom) [2]. Unlike [6], which also estimates the extent of NBTI-induced delay degradation in digital circuits, we consider the fact that the threshold voltage can recover back partially during annealing, and incorporate these into the calculations. We also mathematically prove (for the first time), the observed phenomenon of frequency independence for periodic square waveforms [2], [3], [7], [8]. We also propose a novel method based on signal probabilities and activity factors (SPAF method) of nodes in digital circuits, to quantify the NBTI impact. A look up table of signal probability versus threshold voltage is built, and this is used to estimate the delay of the gates in the circuit, during static timing analysis. This method is used to calculate the increase in delay due to NBTI, on a set of standard combinational benchmark circuits.

II. Solution to the Reaction-Diffusion Model

The Reaction-Diffusion (R-D) model has been used in [2]–[5] to explain the NBTI effect in present day PMOS devices. According to the model, the rate of generation of interface traps initially depends on the rate of dissociation of the Si-H bonds (which is controlled by the rate constant, k_f) and the local self-annealing process (which is governed by the rate constant, k_r). This constitutes the reaction phase in the R-D model. Thus,

$$\frac{dN_{IT}}{dt} = k_f[N_0 - N_{IT}] - k_r N_{IT} N_H^0 \tag{1}$$

where N_{IT} is the number of interface traps, N_0 is the maximum density of $Si-H$ bonds and N_H^0 is the hydrogen density at the $Si-SiO_2$ interface. After sufficient trap generation, the rate of generation of traps is limited by the diffusion of hydrogen. At the interface, it follows the equation:

$$\frac{dN_{IT}}{dt} = -D\frac{dN_{H_2}}{dx} \tag{2}$$

while, the diffusion of hydrogen into the oxide is given by:

$$\frac{dN_{H_2}}{dt} = D\frac{d^2N_{H_2}}{dx^2} \tag{3}$$

where N_{H_2} is the concentration of hydrogen molecules at a distance x from the interface at time t, (while $N_{H_2}^0$, at the interface) and D is the diffusion of hydrogen species. This constitutes the diffusion phase in the R-D model.

We now present the analytical solution of the R-D model assuming that alternate periods of stress and relaxation, each of equal duration t_0, are applied to the gate of a PMOS device, whose source and bulk are tied to V_{dd} while the drain is grounded (Fig. 1).

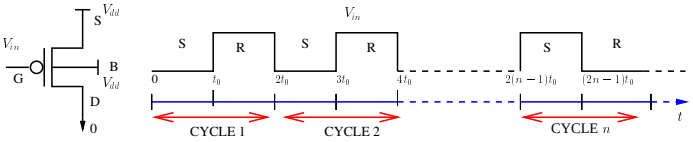


Fig. 1. Input waveform applied to the gate of the PMOS transistor to simulate alternate stress (S) and relaxation (R) phases of equal duration t_0.

Four different cases arise in the model, namely the first stress phase, which occurs from time $t = 0$ to t_0, ($t = 0$ corresponds to the time at which stress is first applied, and the device is unstressed for all $t < 0$), the first relaxation phase which occurs from time t_0 to $2t_0$, the second and subsequent stress phases, and the second

and subsequent relaxation phases. The varying physical mechanisms and the boundary conditions in each of these phases, as well as the dependence on history effects require them to handled separately. Our analytical solution for the first stress and relaxation phases is largely consistent with [3]–[5]. The extension of the analytical model to the subsequent stress/relaxation phases, is an entirely new contribution of this paper. Due to space constraints, the complete derivation for each of these four cases is omitted, and the final analytical expressions are provided below:

- *First Stress Phase*: The trap generation during the first stress phase is given by:

$$N_{IT}(t) = \left(\frac{k_f N_0}{k_r}\right)^{\frac{2}{3}} \left(2k_H^2 D t\right)^{\eta} = k_{IT}\left(D_H t\right)^{\eta} \quad (4)$$

  where $k_{IT} = \left(\frac{k_f N_0}{k_r}\right)^{\frac{2}{3}}$, $D_H = 2k_H^2 D$, (k_H is the rate at which two hydrogen atoms can combine to form a hydrogen molecule), and $\eta = \frac{1}{6}$ for the case of neutral H_2 diffusion. Thus, at $t = t_0$, $N_{IT}(t_0) = k_{IT}(D_H t_0)^{\frac{1}{6}}$.
- *First Relaxation Phase*: The number of interface traps taking into account annealing of bonds, during the first recovery phase is given by:

$$N_{IT}(t_0 + t) = \frac{N_{IT}(t_0)}{1 + \sqrt{\frac{\xi t}{t_0 + t}}} \quad (5)$$

  where ξ indicates the nature of backward diffusion (two-sided or one-sided). Theoretically, $\xi = 0.5$ for double sided diffusion, where as empirically, its value is found to be ≈0.58. At $t = t_0$, i.e., at the end of the first recovery phase, we have $N_{IT}(2t_0) = \frac{2}{3}N_{IT}(t_0)$.
- *Second and Subsequent Stress Phases*: The generalized equation for the number of interface traps during the second and subsequent stress phases is given by:

$$N_{IT}(2kt_0 + t) = \left(\frac{t}{t_0} + \left(\frac{N_{IT}(2kt_0)}{N_{IT}(t_0)}\right)^{\frac{1}{\eta}}\right)^{\eta} N_{IT}(t_0) \quad (6)$$

  At $t = t_0$, we have

$$N_{IT}((2k+1)t_0) = \left(1 + \left(\frac{N_{IT}(2kt_0)}{N_{IT}(t_0)}\right)^{\frac{1}{\eta}}\right)^{\eta} N_{IT}(t_0) \quad (7)$$

- *Second and Subsequent Relaxation Phases*: The equation for the second and subsequent recovery phases is given by:

$$N_{IT}((2k-1)t_0 + t) = \frac{N_{IT}((2k-1)t_0) + N_{IT}((2k-2)t_0)\sqrt{\frac{\xi t}{t_0 + t}}}{1 + \sqrt{\frac{\xi t}{t_0 + t}}} \quad (8)$$

  At the end of the recovery phase, we have

$$N_{IT}(2kt_0) = \frac{2}{3}N_{IT}((2k-1)t_0) + \frac{1}{3}N_{IT}(2(k-1)t_0) \quad (9)$$

The analytical solution of the R-D model for the first two cycles is plotted in Fig. 2. The curve marked as "DC stress" corresponds to the case where the device is stressed continuously, while "AC stress" corresponds to the case, as shown in Fig. 1, i.e., stress and relaxation applied alternatively. The simulation values are compared with the experimental data shown in circles (obtained from Fig. 20 of [7]). Our simulation results for the AC stress case, match with the experimental results, thereby validating the correctness of our analytical solution. The exact shape of the waveform shows a good, but not a perfect match with the experimental results. However, the values at the end of the stress and the relaxation phases closely match the experimental data, and hence captures the overall transient NBTI-action effectively.

Defining s_k as the scaling factor relative to $N_{IT}(t_0)$ at time kt_0, ($s_k = N_{IT}(kt_0)/N_{IT}(t_0)$) we obtain the following equation for even

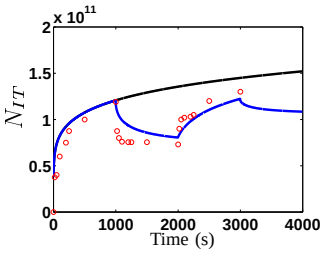


Fig. 2. Analytical solution to the R-D model for the first two cycles and comparison with experimental data from [7].

or odd values of k, (i.e., for the alternate stress or recovery phases of equal duration t_0) as:

$$s_k = \begin{cases} 0 & k = 0 \\ 1 & k = 1 \\ (1 + s_{k-1}^{\frac{1}{\eta}})^{\eta} & k > 1,\ k \text{ odd} \\ \frac{2}{3}s_{k-1} + \frac{1}{3}s_{k-2} & k > 1,\ k \text{ even} \end{cases} \quad (10)$$

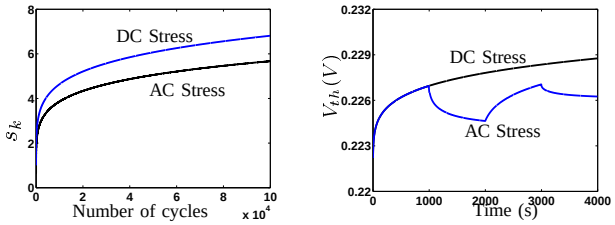
It must be noted that the above set of equations holds good for the neutral H_2 molecular diffusion case, where $\eta = \frac{1}{6}$ as well as the H atom diffusion case, where $\eta = \frac{1}{4}$ and $N_{IT}(t_0) = \sqrt{\frac{k_f N_0}{k_r}}\left(Dt_0\right)^{\frac{1}{4}}$ [3].

The values for the $\eta = \frac{1}{6}$ (H_2 diffusion) case are plotted in Fig. 3(a). Since the data is plotted for a large number of cycles, the stress and relaxation transients are not easy to discern, and the AC stress curve appears to be smooth.

The generation of interface traps due to NBTI causes a shift in the transistor threshold voltage, given by [6] as,

$$\Delta V_{th} = -\frac{(m+1)qN_{IT}}{C_{ox}} \quad (11)$$

Thus, the effect of N_{IT} on V_{th} is linear in nature. The threshold voltage is plotted for the first four phases (first and second stress and relaxation phases) of an AC stress case, and also for the DC stress case in Fig. 3(b). The plot is similar to that seen in [1], [3], [8], which use numerical solutions to estimate the V_{th} shift.



(a) Plot showing s_k for DC and AC stress.

(b) V_{th} shift for DC and AC stress.

Fig. 3. Simulation results showing N_{IT} and V_{th} for DC stress and AC stress. Note that s_k is linearly related to V_{th}.

III. Frequency Independence

An important requirement of any physical model for NBTI [3], is that it should be able to explain the phenomenon of frequency independence, observed over a wide range of frequencies [2], [3], [7], [8]. Frequency independence implies that for any two periodic waveforms with frequencies f_1 and f_2, and the same duty cycle, the number of interface traps generated at any time t, such that $t \gg \frac{1}{f_1}$ and $t \gg \frac{1}{f_2}$, is the same. The concept of frequency independence has been widely demonstrated through experiments using periodic square

waveforms of different frequencies. While there have been varying results about the range of frequencies over which this phenomenon has been observed, experiments have consistently shown that for frequencies less than 10MHz [3], this is true.

We now provide a mathematical proof for the special class of periodic waveforms, namely square waveforms (The proof holds good for rectangular waveforms as well.). Consider two square waveforms A and B, as shown in Fig. 4. Let the time period (T) of A be denoted as t_{0_1}, while the time period of B is t_{0_2}. The duty cycle of both these waveforms is 50% (on time = off time = $\frac{T}{2}$). Let these waveforms be applied to the PMOS device separately, up to a certain time t, such that t is a large integral multiple of t_{0_1} and t_{0_2}. In other words, $t = k_1 t_{0_1} = k_2 t_{0_2}$, k_1 and k_2 being sufficiently large. Further, let $t_{0_1} < t_{0_2}$, and hence $k_1 > k_2$. Let the number of interface traps after time t for the two cases be denoted as $N_{IT}(t_{0_1} k_1)$ and $N_{IT}(t_{0_2} k_2)$, respectively. By "frequency independence", we imply:

$$N_{IT}(t) = N_{IT}(t_{0_1} k_1) = N_{IT}(t_{0_2} k_2) \tag{12}$$

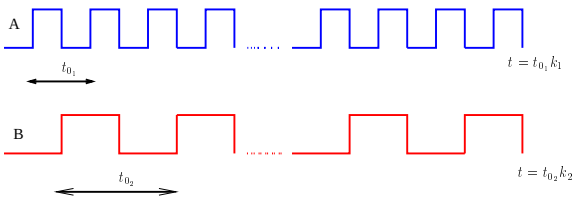


Fig. 4. Figure showing two square waveforms with different time periods but the same duty cycle (50%).

The above equation can be proved mathematically using the expressions for s_k, developed in the previous section. From (10):

$$\begin{aligned} s_k^6 &= s_{k-1}^6 + 1 \\ s_{k-1} &= \frac{2}{3} s_{k-2} + \frac{1}{3} s_{k_1 - 3} \\ s_{k-2}^6 &= s_{k-3}^6 + 1 \end{aligned} \tag{13}$$

It can be shown that for large values of k, the above set of equations can be simplified to:

$$s_k^6 \approx s_{k-2}^6 + \frac{2}{3} \tag{14}$$

The proof of the above approximation is omitted due to lack of space. From (14), for some $m < k$, we can write

$$s_k^6 \approx s_m^6 + \frac{2}{3} \frac{(k-m)}{2}. \tag{15}$$

Choosing k first as k_1, and then as k_2, such that $k_1 \gg m$ and $k_2 \gg m$, we can write:

$$\frac{s_{k_1}^6 - s_m^6}{s_{k_2}^6 - s_m^6} \approx \frac{k_1 - m}{k_2 - m} \tag{16}$$

Since k_1 and k_2 are $\gg m$, and $s_{k_1}, s_{k_2} > 1$, it follows that $s_{k_1}^6 \gg s_m^6$, $s_{k_2}^6 \gg s_m^6$, and the above equation can be approximated as:

$$\left(\frac{s_{k_1}}{s_{k_2}} \right)^6 \approx \frac{k_1}{k_2} \tag{17}$$

Now, we can write N_{IT} as:

$$N_{IT}(t_{0_1} k_1) = s_{k_1} N_{IT}(t_{0_1}) = s_{k_1} k_{IT} (D_H t_{0_1})^{\frac{1}{6}} \tag{18}$$

$$N_{IT}(t_{0_2} k_2) = s_{k_2} N_{IT}(t_{0_2}) = s_{k_2} k_{IT} (D_H t_{0_2})^{\frac{1}{6}} \tag{19}$$

Therefore, using (17), we have

$$\frac{N_{IT}(t_{0_1} k_1)}{N_{IT}(t_{0_2} k_2)} \approx \left(\frac{k_1}{k_2} \right)^{\frac{1}{6}} \left(\frac{t_{0_1}}{t_{0_2}} \right)^{\frac{1}{6}} \tag{20}$$

Since $t_{0_1} k_1 = t_{0_2} k_2$, we have

$$N_{IT}(t_{0_1} k_1) = N_{IT}(t_{0_2} k_2) = N_{IT}(t).$$

IV. Signal Probability and Activity Factor based solution to the R-D Model (SPAF method)

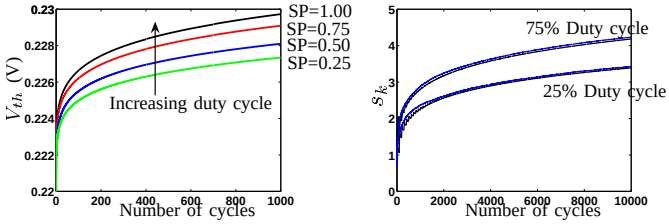
While the NBTI-impact has been analyzed in Sections II-III for a square wave, such waveforms are rarely seen in digital circuits, due to the random distribution of node probabilities. We now present a methodology to estimate the NBTI-induced V_{th} degradation of a PMOS device, when a random aperiodic waveform is applied to its gate. This method, which we call the SPAF (Signal Probability and Activity Factor) method, is based on *signal probability* (SP), i.e., the probability that a node is high or low, and *activity factor* (AF), i.e., the probability that a node toggles every phase, with respect to a reference clock. We first explain the underlying idea behind the SPAF method using simple square waveforms.

A. AF Independence and SP Dependence of Trap Generation

In this subsection, we show that the extent of trap generation is independent of the activity factor (AF) of the signal and depends on the signal probability only (SP). We first elucidate this using two periodic square waveforms of different frequencies.

Let us consider two square waveforms of frequencies, say f_1 =1Hz and f_2 = 100Hz. Comparing the two waveforms with a reference clock of f = 100Hz, the activity factors (AF) and signal probabilities (SP) of these waveforms over a period of time can be computed as: AF_1 = 0.01, AF_2 = 1, SP_1 = 0.5, and SP_2 = 0.5. Using (12), it can be deduced that the interface trap density, calculated at some large time t, is the same for both these waveforms. Hence, we conclude that the extent of trap generation for any two waveforms with identical signal probabilities is independent of their activity factors. Intuitively, this is true because for the signal with a higher activity factor, although fewer traps are generated in each cycle, there are larger number of cycles, thereby leading to the same number of interface traps.

However, the dependence of the trap generation on the signal probability (for two waveforms with equal time period) is rather obvious, since higher on-times imply larger amounts of stress, and lesser amounts of recovery. As seen in Fig. 5(a), four waveforms with the same frequency and different stress duty cycles (0.25, 0.5, 0.75, and 1) are considered and the number of traps generated is plotted for 1000 cycles. Expectedly, there is considerable difference in the final values of the four curves.



(a) (b)

Fig. 5. (a): Signal probability dependency of trap generation shown for four waveforms of equal frequency but varying duty cycles. (b): Simulations for 25% and 75% duty cycle waveforms showing the SPAF method.

B. SPAF Method

The SPAF method helps to convert a random aperiodic signal to an equivalent deterministic waveform, based on its statistical information (SP). Such a transformation is essential in order to perform temporal simulation of circuits, since the exact input waveforms cannot be determined. Since the interface trap density is independent of the AF of a signal, the crux of the SPAF method is to use the signal probabilities of any given node, computed using logic simulators or otherwise. The SP information can now be used to compute an equivalent rectangular periodic waveform with the same SP value, as shown in Fig. 6. Such a transformation is equivalent to representing a 100Hz square waveform by a 1Hz square waveform, both of which have the same SP. The validity of this transformation is based on

the frequency independence property proved in the previous section, since both these waveforms generate the same number of interface traps.

Let the total time period of this new waveform be k cycles, such that it is low for m cycles and high for $k-m$ cycles (Fig. 6). Let n indicate the number of such periods, each of duration k. We can determine the number of interface traps generated, using (6) and (8), for the stress and the relaxation phases respectively. Using the s_k notation, these can be simplified as:

$$s_{nk+i} = \begin{cases} (i + s_{kn}^6)^{\frac{1}{6}} & nk < i \leq nk+m \\ \frac{s_{nk+m} + s_{nk}\left(\frac{i}{2(m+i)}\right)^{0.5}}{1+\left(\frac{i}{2(m+i)}\right)^{0.5}} & nk+m < i \leq (n+1)k \end{cases} \quad (22)$$

For the H_2 diffusion case, (10) can be obtained as a special case of (22) by using $k=2$ and $m=1$.

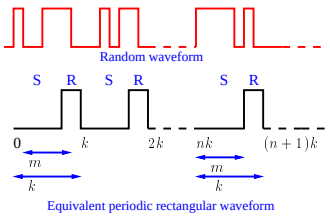


Fig. 6. SPAF method to convert a random waveform (with signal probability $= SP$) to a periodic rectangular waveform with equivalent stress duty cycle ($\frac{m}{k} = SP$).

The SPAF method of equivalent waveform construction is verified for two random waveforms of $SP = 0.25$ and $SP = 0.75$. The samples are accumulated over 10000 cycles. Equivalent rectangular pulse waveforms with $k = 100$ cycles, and $n = 100$ are reconstructed. The total number of interface traps are calculated at the end of 10000 cycles, using (22). The results, plotted in Fig. 5(b), show the number of traps generated for the actual waveform (Monte-Carlo simulation) and the SPAF method based solution. The two curves practically coincide, thereby validating the SPAF method of equivalent waveform construction. The SPAF method can reduce a random aperiodic signal to an equivalent periodic rectangular waveform, and hence, can decrease the amount of computation, without loss of accuracy. This helps is performing quick simulations in a computationally efficient manner, as described in the next section.

V. Impact of NBTI on Circuit Delays

In this section, we present the simulation methodology to compute the delay degradation of ISCAS85 benchmarks, and the simulation results. The standard cell library used for synthesis consists of 5 NOT gates, 5 BUF gates, 3 NAND2 gates, 3 NAND3 gates, 3 NOR2 gates, and 3 NOR3 gates of different sizes. The circuits are synthesized using a a 70nm PTM [9] model and circuit simulations are performed at $T = 105^\circ C$.

Since it is impossible to know the exact nature of stress and relaxation on each PMOS transistor in a digital circuit, we precompute the statistical information (SP and AF) of the various nodes in the digital circuit. The SPAF method is used to convert these probabilistic waveforms into deterministic periodic signals, by faithfully preserving the signal probabilities. Assuming the clock frequency to be 10MHz, (since 10MHz is the onset of frequency dependence of trap generation [3]), we use the SP values to represent these random signals at every node of the digital circuit, as rectangular waveforms of frequency 1Hz, such that the duty cycle is equal to the computed signal probabilities. Note that we choose the equivalent waveform to be of frequency 1Hz in order to reduce the amount of computation*. Although simulations using the R-D model have been shown to match the experimental findings up to 10MHz, for higher frequencies, the dependency of trap generation on the frequency is rather weak [3], [10], and hence the results do not change significantly, for gigahertz operation.

*Choosing any frequency between 1Hz-10MHz gives the same result, because of frequency independence. However, choosing a value of less than 1Hz leads to a loss of accuracy.

TABLE I
Delay Degradation for ISCAS benchmarks

	Nominal Delays		NBTI Delays		
Benchmark	Rise (ps)	Fall (ps)	Rise (ps)	Fall (ps)	% Increase
C1355	667	669	717	730	7.50
C1908	982	975	1043	1064	6.21
C2670	701	709	761	771	8.56
C3540	1226	1229	1340	1339	9.30
C432	883	897	960	966	8.72
C499	684	682	745	736	8.92
C5315	1045	1048	1134	1139	8.52
C6288	3552	3556	3867	3868	8.87
C880	619	617	671	667	8.40
Average					8.33

We now use (11) and (22), and compute the number of traps and the threshold voltage degradation for the circuit whose nodal waveforms are represented by these deterministic rectangular signals, for 3×10^8 cycles, i.e., 3×10^8s (≈ 10 years). A look-up table of SP versus V_{th} is built and the library gate delays are characterized as a function of V_{th}. These values are used during static timing analysis, and the new circuit delays in the presence of temporal degradation are computed. The results are tabulated in Table I. The rise and fall delays (arrival times at the most critical output nodes) are computed at time $t = 0$s for the nominal case, and at $t = 3 \times 10^8$s for the NBTI-affected case. The percentage increase in delays is plotted in the final column and an average degradation of 8.33% is seen for these combinational benchmarks. Since the benchmark circuits consist of mostly inverting gates, both the critical paths leading to an output rise as well as an output fall contain pull-up logic with NBTI affected PMOS transistors. Expectedly, the rise and fall arrival times show a similar extent of increase in delay, due to NBTI.

VI. Acknowledgment

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