EE 4363/CSci 4203

Computer Architecture & Machine Organization [4 Credits]

Spring 2016

1 Course Overview

	T/Thu 09:45-11:00
Coordinates:	Ackerman 319
	https://ay15.moodle.umn.edu/course/view.php?id=12553

Instructor:

Ulya Karpuzcu
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Teaching Assistant:

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Office Hours:	Thu 2-3pm	Mon 2-3pm

Objectives: We are going to cover basic principles of computer architecture design. Subject to limitations of the underlying process technology, architectural design practices emerge in tailoring computer systems to specific application domains.

Prerequisites: EE 2361 or equivalent. A solid understanding of logic design principles is expected, but basics will be covered in class.

Reference Material: "Computer Organization and Design: The Hardware/Software Interface" by Hennessy/Patterson, revised 4^{th} Edition represents the main textbook. "Designing Computer Systems with Verilog" by Lilja/Sapatnekar is recommended.

Exams: We will only have one exam. The exam may be designated as an open book/notes/... take-home to be submitted 24 hours after the release of questions (the exam dates are to be interpreted as release dates in this case).

Exam: Thursday, May 12, 08:00-10:00

Homeworks: There will be 4 homeworks. Homeworks may include thought-provoking open-ended challenge questions (as bonus).

Machine Problems: You will need a Verilog simulator for the machine problems. As an open source tool, we have Icarus Verilog available in CSE labs. You can also have the following tools installed on your personal computer:

- Icarus Verilog (recommended):
  `http://iverilog.icarus.com`
- ModelSim PE Student Edition:
  `http://www.mentor.com/company/higher_ed/modelsim-student-edition` (free for use by students in their academic coursework). You may need to register.

- Xilinx ISE WebPACK:
  `http://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.htm` (free version of Design Studio). You may need to register.

	Exam	30%
GRADING:	Machine problem ($\times 4$)	30%
	Homework ($\times 4$)	40%

MECHANICS:

- Regarding academic integrity and scholastic dishonesty, according to the Office for Student Conduct and Academic Integrity (OSCAI), "Academic integrity is essential to a positive teaching and learning environment. All students enrolled in University courses are expected to complete coursework responsibilities with fairness and honesty. Failure to do so by seeking unfair advantage over others or misrepresenting someone elses work as your own, can result in disciplinary action. The University Student Conduct Code defines scholastic dishonesty as follows: Scholastic Dishonesty: submission of false records of academic achievement; cheating on assignments or examinations; plagiarizing; altering, forging, or misusing a University academic record; taking, acquiring, or using test materials without faculty permission; acting alone or in cooperation with another to falsify records or to obtain dishonestly grades, honors, awards, or professional endorsement." applies. **Independent of the scope (be it a homework assignment, exam, ...), any conduct leads to F as the immediate final grade.**
- The students are expected to attend all class meetings. Office hours are not designated to serve as make-up lectures.
- All assignments are due at the beginning of class, on the designated due date. Late assignments will receive a reduction of 20% for each day they are late, except for documented illnesses and family emergencies.
- Any question or concern about grading must be communicated to the TA or the instructor within one week after the return of the exam or assignment concerned.
- You can work in groups to discuss assignments, as long as the submission reflects your own work.
- If the students fail to submit all of the homeworks, their final will not be graded.
- If the students fail to submit all of the machine problems, their final will not be graded.
- If the students fail to take the midterm, their final will not be graded.
- Any non-submitted or non-graded item will be processed with a grade of 0.
- Regarding incomplete grades, according to University Senate policy, "The I grade shall be assigned at the discretion of the instructor when, due to extraordinary circumstances, the student was prevented from completing the work of the course on time. The assignment of an I requires a written agreement between the instructor and student specifying the time and manner in which the student will complete the course requirements. In no event may any such written agreement allow a period of longer than one year to complete the course requirements." applies. An "I" will only be assigned if less than 15% of the course remains to be completed. In such a case, the "extraordinary circumstances" must be properly documented.
- Any student with disabilities to affect their ability to participate fully in class or to meet all course requirements is encouraged to notify the instructor so that appropriate accommodations can be timely arranged.

2 COURSE OUTLINE

- **Impact of Technology on Computer System Design:** Historical perspective and future trends.
- **Quantitative Analysis of Computer Systems:** Metrics and benchmarks.
- **Instruction Set Architecture:** Assembly language programming.
- **Computer Microarchitecture:** Pipelining basics, pipeline hazards, instruction-level parallelism.
- **Memory System Design:** Memory hierarchy, cache memory, virtual memory.
- **Computer System Design:** Storage systems, input/output systems, networks.

3 TENTATIVE TIMELINE

Week	Tue	Thu	Assignment	(Main) Reference
1	Impact of Technology	Impact of Technology		H&P Ch. 1
2	Quantitative Analysis	Quantitative Analysis		H&P Ch. 1
3	Instruction Set Architecture	Instruction Set Architecture	HW1 out:Thu	H&P Ch. 2
4	Instruction Set Architecture	Instruction Set Architecture	MP1 out: Thu	H&P Ch. 2
5	Computer Microarchitecture	Computer Microarchitecture	HW1 due: Thu	H&P Ch. 4
6	Computer Microarchitecture	Computer Microarchitecture	HW2 out: Tue MP1 due: Thu	H&P Ch. 4
7	Computer Microarchitecture	Computer Microarchitecture	MP2 out: Thu	H&P Ch. 4
8	Computer Microarchitecture	Computer Microarchitecture	HW2 due: Tue	H&P Ch. 4
9	Computer Microarchitecture	Computer Microarchitecture	MP2 due: Thu MP3 out: Thu	H&P Ch. 4
10	Computer Microarchitecture	Computer Microarchitecture	HW3 out: Thu	H&P Ch. 4
11	Memory Hierarchy Design	Memory Hierarchy Design	MP3 due: Thu MP4 out: Thu	H&P Ch. 5
12	Memory Hierarchy Design	Memory Hierarchy Design	HW3 due: Thu	H&P Ch. 5
13	Memory Hierarchy Design	Memory Hierarchy Design	HW4 out:Thu	H&P Ch. 5
14	Memory Hierarchy Design	Computer System Design	MP4 due:Thu	H&P Ch. 5, 6
15	Computer System Design		HW4 due:Thu	H&P Ch. 6