

# THEORETICAL ESTIMATION OF POWER CONSUMPTION IN BINARY ADDERS

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## ABSTRACT

This paper presents a novel approach for theoretical estimation of power consumption in digital binary adders. Closed-form expressions for power consumption of four different types of binary adders – the ripple-carry adder, the Manchester adder, a multiplexor-based carry-select adder and an efficient tree-based look-ahead adder – are derived in terms of word-length and pre-computed technology-specific energy parameters. These expressions are verified to be accurate to within 1 - 5% by simulation using the HEAT tool.

## 1. INTRODUCTION

This paper proposes a novel theoretical approach for estimation of power dissipation of four different types of binary adders: the ripple-carry adder, the Manchester adder, a multiplexor-based carry-select adder and an efficient tree-based look-ahead adder. Although power consumption of binary adders has been compared by simulations [10], no theoretical method for estimation of power consumption has been presented thus far. To the best of the authors' knowledge, the proposed approach is the first systematic technique for theoretical estimation of power consumption in binary adders.

In this process, power consumption formulations are expressed in terms of the word length and technology-dependent energy parameters. As a first step, component cells are identified and characterized according to input and output transitions e.g., in the case of the ripple-carry adder, carry and sum transitions in the context of full-adder cells present a convenient level of abstraction. The energies associated with these transitions are extracted using SPICE. The analytical aspect of this method proceeds with the determination of probabilities related to the propagation or termination of transition stimuli.

The derivation of these solutions develops from a temporally-discretized model employing element-level abstraction. The formulations are arranged as either closed-form expressions or trivial one-loop procedures. Yet, they attain a level of accuracy approaching that of full-scale simulation. Computational requirements are dramatically minimized with this methodology. Therefore, these formulations are indicated in lieu of simulation whenever the binary adder is selected as the principal target of optimization.

## 2. SPECIFICATION OF THE MODEL

The convenient formulations produced by this method are derived from a general model which employs element-level abstraction to

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This work was supported by DARPA under grant number DA/DABT63-96-C-0050.

avoid technology-specific detail. The only acknowledgment of the underlying technology comes in the form of a series of trivial simulations from which the energies accompanying particular transitions are extracted. Transitions with homogeneous energy consumption and I/O traits are amalgamated into transition classes. The energies associated with these classes appear directly in the final expressions.

Discretizing the computation period imposes conceptual order on the carry-propagation process by aligning switching activity with well-defined temporal references. To abate complexity, distinct phases of operation in which elements share similar properties are determined.

Each structure is statistically scrutinized to obtain interdependent transition probabilities for each unit. In order to mitigate complexity, synchronous switching and a uniform distribution of signal levels are assumed at the inputs of the structure. These requirements do not diminish the validity of relative comparisons of architectures that do not conform to these assumptions.

The hallmark process of the binary adder is propagation. Understanding of it is aided by three conceptual devices. The first – the *hold-state cell* – is defined as any cell which blocks the transmission of switching activity from the preceding to the succeeding bit position. By contrast, the *carry-state cell* always relays such activity. Finally, a *carry chain* is formed by the advent of a contiguous series of carry-state cells. In addition, it will be necessary to distinguish between carry-state and hold-state cells in the current computation period and the vestigial carry-state and hold-state cells from the previous period whose propagation-stabilized outputs are extant at the beginning of the new period.

## 3. RIPPLE-CARRY ADDER

Of all binary adder variants, none is more evocative of the least-significant to most-significant sequential pen-and-paper tallying process than the ripple-carry adder illustrated in Figure 1. The full-adder cell is considered elemental for this architecture. It is found that transition occurrences on this element can be categorized into four classes expending energies of  $e_c$ ,  $e_s$ ,  $e_{cs}$  and  $e_n$ , where the subscript, with the exception of  $n$  which refers to the case with no output transition, denotes the output(s) which switched.

The ripple-carry computation period can be decomposed into two phases: the generation phase and the propagation phase. The one-time-slot generation phase is initiated immediately upon the start of a new computation period, while the propagation phase spans the remainder of the computation period. In the generation phase either or both of the external  $x$  and  $y$  inputs may change while the

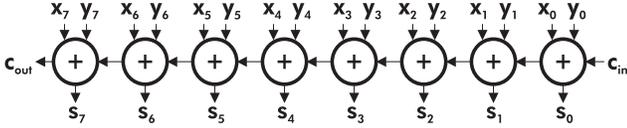


Figure 1: Structure of the ripple-carry adder.

$c_{in}$  inputs remain stable. The propagation phase, however, permits only the  $c_{in}$  inputs to vary. The least-significant cell is an exception, since all three inputs may change in the generation phase and none thereafter.

Consider the addition of two  $W$ -bit words. In the generation phase, the probability of each of the four transition types occurring at the least-significant cell position given a uniform distribution on the inputs can be found by inspection of the full-adder truth table. Multiplying those probabilities by the associated energy of the transition classifications results in a total average energy of

$$\frac{1}{16} (5e_{cs} + 3e_s + 3e_c + 3e_n).$$

By inspection of the abbreviated set of permissible transmissions associated with an invariant carry input, the energy expended in the remaining  $W - 1$  cells is found to be

$$\frac{W-1}{8} (2e_{cs} + 2e_s + e_c + e_n).$$

In the propagation phase, hold-state cells as well as the least-significant cell generate a switching disturbance with probability  $\frac{1}{2}$ . For carry-state cells, a switching disturbance will only be instigated if the vestigial cell in the same position assumed the hold-state. Overall, the probability of switching is  $\frac{1}{4}$ . It can be demonstrated that only transitions with associated energy  $e_{cs}$  and  $e_s$  can occur in carry-state cells and hold-state cells, respectively.

Given the switching probabilities above and the understanding that input toggling will be transmitted to the terminus of the chain, it follows directly that a carry chain of length  $v$  preceded by a hold-state or least-significant cell must induce

$$\frac{1}{4}v + \frac{1}{2} = \frac{1}{4}(v+2)$$

switching instances on the cell succeeding the chain. Recalling the allowed transition energies and accounting for carry chains ranging from length 0 to  $p-2$ , for every active position,  $p$ , the total energy over all active cells is found to be

$$(e_{cs} + e_s) \sum_{p=2}^W \left( \frac{1}{8} \sum_{v=0}^{p-3} (v+2) \frac{1}{2^{v+1}} + \frac{1}{4} \frac{1}{2^{p-2}} \right) = \frac{1}{8} \left( 3w - 5 + \frac{1}{2^{w-2}} \right) (e_{cs} + e_s).$$

Summing the generation and propagation phase expressions results in the complete expression for the ripple carry adder, which is

$$\frac{1}{16} \left( 2e_{cs} + \left( 10W - 11 + \frac{1}{2^{w-3}} \right) (e_{cs} + e_s) \right) + \frac{1}{16} (2W + 1) (e_c + e_n).$$

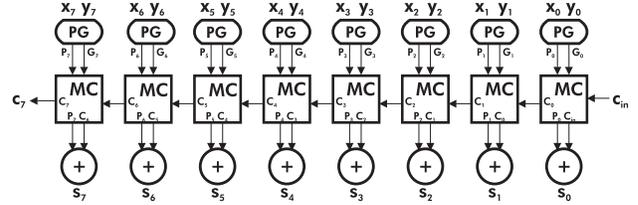


Figure 2: Structure of the Manchester adder

The accuracy of this expression has been determined through comparison with simulation results. Reliable energy consumption characterizations for the prototypical elements have been obtained from SPICE. Subsequently, these results were distilled into the four energy categorizations identified earlier. Independently, a fast and accurate energy analysis tool [13] was employed to compute the aggregate power consumption of the circuit. The formula shown above agrees with the simulation to within 4%, as shown in Table 1.

Table 1. Power consumption of ripple-carry adder.

Length	Simulation ( $\mu\text{W}$ )	Theory ( $\mu\text{W}$ )	Error
1	11.17	10.91	-2.37%
2	27.33	268.3	-1.84%
4	64.69	629.4	-2.71%
6	104.2	101.0	-3.06%
8	142.1	139.5	-1.86%
10	185.3	178.1	-3.85%
12	225.2	216.8	-3.71%
14	264.3	255.5	-3.36%
16	303.5	294.1	-3.09%
24	463.3	448.9	-3.12%
32	625.0	603.6	-3.43%
40	782.3	758.3	-3.07%
48	944.1	913.0	-3.30%
56	1103	1068	-3.21%
64	1265	1222	-3.34%

#### 4. MANCHESTER ADDER

The Manchester adder illustrated in Figure 2 is unique among the fast adders in the sense that it derives its speed advantage from performance improvements to its constituent cells, rather than a more efficient interconnection scheme. The hardware can be divided into three stages: the PG-cell stage, the Manchester-cell stage and the sum-cell stage. In the PG-cell stage, energies  $e_{pg}$ ,  $e_p$ ,  $e_g$  and  $e_n$  corresponding to changes on both, one, or none of the outputs are identified. In the Manchester stage, energies  $e_{mcp}$ ,  $e_{mp}$ ,  $e_{mc}$  and  $e_{mn}$  represent the dissipations associated with changes on the  $p$  input and the  $c$  output in a manner consistent with the previous notational schemes. Finally, the sum-cell stage is described by a single energy,  $e_s$ , associated with any change on the inputs.

The energy of the PG stage can be developed by inspection of the truth table as

$$\frac{w}{8} (2e_{pg} + 2e_p + e_g + e_n).$$

A distinct generation phase and a propagation phase are apparent in the Manchester and sum stages. From inspection of the truth

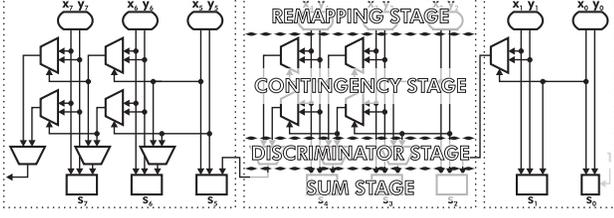


Figure 3: Structure of the multiplexor-based carry-select adder.

tables, the energy expended in the generation phase can be derived as

$$\frac{w-1}{8} (2e_{mcp} + e_{mc} + 2e_{mp} + e_{mn} + 4e_s) + \frac{1}{8} (2e_{mcp} + 2e_{mc} + 2e_{mp} + e_{mn} + 4e_s).$$

Due to similarities between this architecture and the previous, the propagation phase energy can be summarily written by replacing the transition-energy parameters in the ripple-carry result of the same phase. This leads to an energy of

$$\frac{1}{8} \left( 3w - 5 + \frac{1}{2^{w-2}} \right) (e_{mc} + e_{mn} + 2e_s).$$

Thus, the total energy dissipated in the Manchester structure can be arranged as

$$\frac{w}{8} (2e_{pg} + 2e_p + e_g + e_n + 2e_{mcp} + 2e_{mp}) + \frac{1}{8} \left( 4w - 5 + \frac{1}{2^{w-2}} \right) (e_{mc} + e_{mn} + 2e_s) + \frac{1}{8} e_{mc} + \frac{w}{4} e_s.$$

Following the practice outlined in the previous section, simulations were performed. Agreement to within better than 9% was observed as shown in Table 2.

Table 2. Power consumption of Manchester adder.

Length	Theory ( $\mu\text{W}$ )	Simulation ( $\mu\text{W}$ )	Error
4	53.39	56.47	-5.77%
8	115.0	105.5	8.29%
16	239.2	237.2	0.83%
32	487.5	456.9	6.28%
38	735.9	675	8.27%
64	984.2	898.5	8.71%

## 5. CARRY-SELECT ADDER

A uniquely efficient implementation of the carry-select constructed entirely of multiplexors can be formed by exploiting the intrinsic degeneracy in the truth table of a full adder. The structure is illustrated in Figure 3, where four stages are visible. The details of this structure can be found in [12] and [7]. The “blocking” or propagation-isolation tactic employed by this scheme is typical of fast adders and will provide a convenient perspective for this analysis.

To begin, the re-mapping stage, which re-assigns a redundant input-output association can be verified by inspection to consume energy

$$\frac{1}{8} (e_0 + 4e_1 + e_2) w_b,$$

where  $w_b$  is the block length and  $\sum_{b=1}^B w_b = W$ . Here the subscripts of the energy parameters indicate the number of toggled outputs.

### 5.1. Contingency Stage

This structure achieves performance gains by pre-calculating alternative propagation chains. Although each chain is functionally equivalent to the ripple-carry process, the distribution on carry input of the least-significant cell differs appreciably. In the generation phase, this results in a dissipation of

$$\frac{3}{64} (5e_t + 5e_{ts} + 3e_s) + \frac{3}{8} (w_b - 2) e_t$$

where the three energy parameters represent the energy of an output transition only, an output transition accompanying a select-line change and a select-line change alone, respectively. In the propagation phase, the total energy consumption amounts to

$$\frac{1}{32} \left( 12w_b - 33 + \frac{9}{2^{w_b-2}} \right) (e_{ts} + e_s).$$

Thus, for both chains, the total required energy is, on average,

$$\frac{3}{32} \left( 8w_b - 19 + \frac{24}{2^{w_b}} \right) (e_{ts} + e_s) + \frac{6}{32} e_{ts} + \frac{3}{32} (8w_b - 11) e_t,$$

except for the simplified first block, which dissipates only

$$\frac{1}{16} \left( 6w_b - 13 + \frac{1}{2^{w_b-4}} \right) (e_{ts} + e_s) + \frac{2}{16} e_{ts} + \frac{3}{16} (2w_b - 3) e_t.$$

### 5.2. Discriminator and Sum Stages

The third stage of the carry-select structure is responsible for selecting between the alternative outputs of the previous stage. Based on the pair-wise characterization of those outputs it can be shown that the number of transitions at position  $p$  is

$$\tau^{(p)} = \frac{3}{4} - \frac{9}{16} 2^{-p} + \gamma^{(p)} = \frac{1}{16} \left( 12 - \frac{9}{2^p} \right) + \gamma^{(p)},$$

where

$$\gamma_b^{(p)} = \begin{cases} \frac{2z_{b-1}}{2^{p+3}} \frac{\tau_{b-1}^{(p)}(n_{b-1})}{z_{b-1}}, & z_{b-1} + 1 < p \\ \frac{(4z_{b-1} - 2p - 1) \tau_{b-1}^{(p)}(n_{b-1})}{2^{p+3} z_{b-1}}, & p \leq z_{b-1} + 1, b = 1 \\ \frac{(4z_{b-1} - 2p + 1) \tau_{b-1}^{(p)}(n_{b-1})}{2^{p+3} z_{b-1}}, & p \leq z_{b-1} + 1, b > 1 \end{cases}$$

and  $z$  is defined by the recursive relation

$$z_b = \begin{cases} w_b - 1 & b = 0 \\ \max(z_{b-1}, w_b - 1) & b = 1 \\ \max(z_{b-1} + 1, w_b - 1) & b > 1 \end{cases}.$$

Determining the switching activity of the first block as

$$\frac{3}{4} - \frac{1}{2^{z_1+1}}$$

completes the definition.

Defining  $T_b = \tau_b|_{p=w_b-1}$ , the energy expended by the cell at position  $p$  is determined to be

$$\begin{aligned} & \frac{T_{b-1}}{16p} \left( 12 + (4p-9) \frac{1}{2^p} \right) e_{ts} + \\ & \frac{3(p-T_{b-1})}{16p} \left( 4 - \frac{3}{2^p} \right) e_t - \\ & \frac{T_{b-1}}{16pz_b} \left( (2p-1) z_b \frac{1}{2^{p-1}} - 16pz_b - \frac{6p}{2^{z_b}} + 6p \right) e_s. \end{aligned}$$

Using the previous definitions, the sum stage may be shown to consume energy

$$\frac{1}{8} (4e_1 + e_0) w_b + \frac{1}{2} e_t w_b + \sum_{p=0}^{w_b-1} \tau_b^{(p)} e_{ts}.$$

The figures produced by this formulation are consistent with simulation to within better than 5% as demonstrated in Table 3.

Table 3. Power consumption of carry-select adder.

Block Distrib.	Simul. ( $\mu$ W)	Theory ( $\mu$ W)	Error
2,2,3,4,5	810.0	807.1	0.36%
2,2,3,3,3,3	762.3	767.2	-0.65%
3,3,3,3,4	784.6	783.6	0.13%
4,4,4,4	806.2	804.0	0.27%
4,3,4,5	813.0	804.0	1.11%
5,5,6	830.7	827.2	0.43%
4,2,5,2,3	759.5	771.9	-1.64%
4,3,3,3,3	759.5	764.0	-0.60%
5,3,4,4	776.4	781.7	-0.68%
6,6,4	795.0	804.9	-1.25%
6,5,5	796.9	803.5	-0.82%
2,2,2,2,2,2,2,2	686.4	715.7	-4.28%
5,5,2,2,2	738.9	758.6	-2.68%
8,8	788.0	804.4	-2.08%

## 6. DGB ADDER

The basis of the fastest of the fast adders is the provably optimal binary-tree connection paradigm. The Brent-Kung adder [1], the Montoye adder [9], and the Dozza, Gaddoni and Baccarani (DGB) adder [4] which is analyzed here represent the three extremes of tree-based look-ahead adder design, with the first minimizing fan-out and component count, the second achieving both low latency and component count and the final design accomplishing the simultaneous optimization of fan-out and latency.

Three stages of this design are apparent in Figure 4: the propagate (PG) logic, the historically-titled "O"-operator network, and the sum logic. In the PG stage it is found by inspection that the energy expended in this stage is

$$\frac{1}{8} (e_0 + 3e_1 + 2e_2) (W-1) + \frac{1}{2} e_b,$$

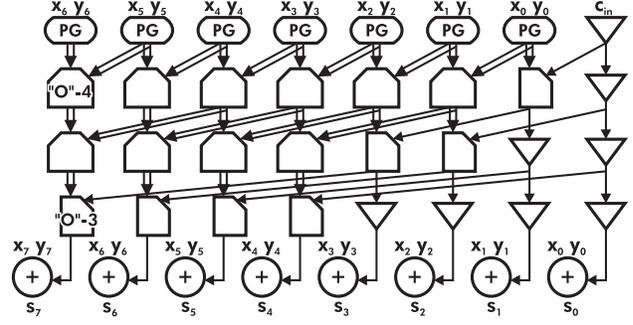


Figure 4: Structure of the DGB tree-based adder.

where  $e_N$  for  $N \in \{0, 1, 2\}$  represents the energy dissipated when  $n$  outputs make a transition and  $e_b$  denotes the energy consumed by a buffer.

The four-input "O"-operators produce switching energies of  $e_p$ ,  $e_g$ ,  $e_{pg}$  and  $e_n$ , where subscripts  $p$ ,  $g$  and  $pg$  signify transitions on the outputs with the same designation and  $n$  denotes a lack of variation on both outputs. The three-input operators dissipate energy  $e_c$  when an output change is induced and energy  $e_{nc}$  when the output does not react. Since the PG cells dwell in the state with a high level on the  $g$  output with probability  $\frac{1}{4}$ , the probability of a high level at depth  $k$  in the "O"-operator network can be shown to obey the relation

$$P_g^{(k)} = \frac{2^{2k} - 1}{2^{2k+1}}.$$

Consequently, the probabilities of transition events on the four-input cells can be written in terms of  $P_g^{(k-1)}$  as shown in Table 4 where the subscript and superscript have been omitted for simplicity. Three-input cells consume energy  $e_c$  with probability  $\frac{1}{2}$  and  $e_{nc}$  with probability  $2P - 3P^2$ .

Table 4. Probabilities of output transition events.

Energy event	Probability
$e_n$	$4P^2 - 12P^4$
$e_g$	$8P^2 - 16P^3 + 8P^4$
$e_p$	$4P - 20P^2 + 32P^3 - 16P^4$
$e_{pg}$	$4P - 20P^2 + 32P^3 - 16P^4$

Multiplying by the number of elements of each kind at every level of iteration and summing over all levels produces the expression of the energy required on average by the "O"-operator network as

$$\begin{aligned} & \sum_{k=1}^{\lceil \log W \rceil} \left( (W-2^k) \left( P_{e_n}^{(k)} e_n + P_{e_g}^{(k)} e_g + P_{e_{pg}}^{(k)} (e_p + e_{pg}) \right) + \right. \\ & \left. 2^{k-1} \left( \frac{1}{2} (e_c + e_b) + P_{e_{nc}}^{(k)} e_{nc} \right) \right) + \\ & (\lceil \log W \rceil - \lfloor \log W \rfloor) \left( 2^{\lfloor \log W \rfloor} \left( \frac{1}{2} (e_c + e_b) - \right. \right. \\ & \left. \left. P_{e_{nc}}^{\lfloor \log W \rfloor} e_{nc} \right) + W P_{e_{nc}}^{\lfloor \log W \rfloor} e_{nc} \right). \end{aligned}$$

The total energy expended in the sum stage can be written by inspection as

$$\frac{1}{8} (3e_{cs} + 4e_{sum} + 2e_{cout} + e_{ncs} + (W - 1)(7e_s + 3e_{ns})),$$

where  $e_s$  and  $e_{ns}$  indicate the energies corresponding to transitions on the sum-only adder cells, while  $e_{sum}$ ,  $e_{cout}$ ,  $e_{cs}$  and  $e_{ncs}$  refer to the associated energies of full-adder-cell transitions.

The formulation for this adder also demonstrates a high-precision agreement. Theoretical and experimental data are compared in Table 5.

Table 5. Power consumption of DGB adder.

Length	Theory ( $\mu W$ )	Simulation ( $\mu W$ )	Error
2	46.8	49.4	-5.26%
4	110.0	107.8	2.04%
6	191.2	202.7	-5.69%
8	253.1	261.7	-3.29%
10	313.3	323.35	-3.11%

## 7. CONCLUSIONS

A selection of adder structures has been analyzed in the context of a temporally-discretized, high-level model applicable to a broad range of technologies. Computational simulation requirements were demonstrated to be minimal making the resultant formulations particularly well suited to quick and convenient estimation work. Theoretical results were verified experimentally to be of high accuracy.

## 8. REFERENCES

- [1] R. P. Brent and H. T. Kung, "A regular layout for parallel adders," *IEEE Trans. Comput.*, v. C-31, no. 3, pp. 260-264, 1982.
- [2] T. K. Callaway and E. E. Swartzlander, Jr., "Estimating the power consumption of CMOS adders," in *Proc. 11th Symp. Comp. Arithmetic*, pp. 210-219, 1993.
- [3] J. Dobson and G. Blair, "Fast two's complement VLSI adder design," *Electronics Letters*, v. 31, no. 20, 1995.
- [4] D. Dozza, M. Gaddoni, G. Baccarani, "A 3.5ns, 64 bit, carry-lookahead adder," in *Proc. ISCAS '96*, pp. 297-300, 1996.
- [5] R. Ladner and M. Fischer, "Parallel prefix computation," *J. ACM*, v. 27, no. 4, pp. 831-838, 1980.
- [6] T. Lynch and E. Swartzlander, "A spanning tree carry-lookahead adder," *IEEE Trans. Comput.*, v. 41, no. 8, pp 931-939, 1992.
- [7] H. Makino, Y. Nakase, H. Suzuki, H. Morinaka, H. Shinohara, K. Mashiko, "An 8.8ns 54-54 bit multiplier with high speed redundant binary architecture," *IEEE J. Solid State Circuits*, v. 31, no. 6, 1996.
- [8] L. Montalvo, J. Satyanaryana, K. K. Parhi, "Estimation of average energy consumption of ripple-carry adder based on average length carry chains," in *Proc. of IEEE Workshop on VLSI Signal Processing*, 1996.
- [9] R. K. Montoye, "Area-time efficient addition in charge based technology," in *Proc. 18th Design Automation Conference*, pp. 862-872, 1981.
- [10] C. Nagendra, M. Irwin, and R. Owens, "Area-time-power tradeoffs in parallel adders," *IEEE Trans. CAS-II*, v. 43, no. 10, pp.689-702, 1996.
- [11] T. Ngai, "Regular, area-time efficient carry-lookahead adders," *J. Parallel and Dist. Comput.*, v. 3, pp. 92-105, 1986.
- [12] K. K. Parhi, "Fast low-energy VLSI binary addition," in *Proc. of IEEE Int. Conf. on Computer Design*, pp. 676-684, 1997.
- [13] J. H. Satyanaryana and K. K. Parhi, "HEAT: Hierarchical Energy Analysis Tool," in *Proc. 33rd ACM/IEEE Design Automation Conference*, pp. 9-14, 1996.
- [14] S. Winograd, "On the time required to perform addition," *J. ACM*, v. 12, no. 2, pp. 277-285, 1965.
- [15] H. Yung and C. Allen, "Recursive addition and its parameterisation in VLSI," *IEE Proc. Part G*, v. 133, no. 5, 1986.