Fully Integrated Low Phase-Noise VCOs With On-Chip MEMS Inductors

Eun-Chul Park, Yun-Seok Choi, Jun-Bo Yoon, *Member, IEEE*, Songcheol Hong, *Member, IEEE*, and Euisik Yoon, *Member, IEEE*

***Abstract*—We present fully integrated high-performance voltage-controlled oscillators (VCOs) with on-chip microelectromechanical system (MEMS) inductors for the first time. MEMS inductors have been realized from the unique CMOS-compatible MEMS process that we have developed to provide suspended thick metal structures for high-quality (Q) factors. Fully integrated CMOS VCOs have been fabricated by monolithically integrating these MEMS inductors on the top of the CMOS active circuits realized by the TSMC 0.18-μm mixed-mode CMOS process. Low phase noise has been achieved as −124 and −117 dBc/Hz at 300-kHz offset from carrier frequencies of 1 and 2.6 GHz, respectively, in the fabricated single-chip VCOs.**

***Index Terms*—CMOS compatible, inductor, microelectromechanical system (MEMS), monolithic integration, phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

THE voltage-controlled oscillator (VCO) is one of the important components in RF communication systems. The carrier frequency of most RF oscillators is adjusted by a phase-locked loop (PLL) to select one of many channels because a given transceiver is assigned different carrier frequencies at different times [1]. VCOs have been widely used to build RF blocks and have been studied for a long time [2]–[5]. Even though a significant amount of research and work had been carried out, the VCO is still a challenging component among RF designers. It is because more stringent requirements are imposed on VCOs as the need for wireless communications is increasing and new applications are coming into the wireless market at higher frequencies. The major issue in recent VCO research is to achieve monolithic integration of low phase-noise VCOs with low-power consumption at given application frequencies. There have been many attempts to integrate high-performance VCOs into a single chip, including inductors made of top-layer metal interconnection lines available from standard silicon processes such as bipolar junction transistors (BJTs) [6], BiCMOS [7], and CMOS [8], [9]. Among these, CMOS VCOs have drawn high attention because they can easily combine RF parts with baseband blocks that are already available in CMOS technology. Although CMOS technology has been a mainstream process in the digital design community, it has not been considered as an adequate process for RF circuit modules due to its high noise, low operating frequency, and small transconductance. Recently, the demand for system integration in wireless communications has attracted RF designers to build extensive RF circuit blocks using CMOS processes with the help of recent advancement in performance improvement of deep submicrometer CMOS technologies.

In spite of these endeavors, integrated VCOs still have difficulty in emerging into commercial markets. It is because integrated VCOs using standard silicon processes have a hard time with meeting rigorous communication specifications with enough margin due to their relatively poor characteristics of available passive components such as on-chip inductors. Phase noise, one of the major specifications, is directly related with the quality factor (Q) of an LC tank used in VCOs. Generally, the inductors obtained from standard silicon processes cannot provide sufficient Q factors. (Typical Q factors from commercially available silicon processes are less than 12 in 1∼5-GHz range [10], [11]). Therefore, it is required to devise a new way of providing high-Q on-chip inductors in order to intrinsically improve the performance of VCOs.

In this paper, we report low phase-noise VCOs monolithically integrated with on-chip microelectromechanical system (MEMS) inductors. We have integrated suspended spiral MEMS inductors using surface micromachining technology and have achieved high-Q factors over 25 at 1–4 GHz [12], [13]. These suspended MEMS structures can provide high-Q factors by significantly reducing coupling loss to the substrate. Recently, various MEMS technologies have been applied to fabricate high-performance RF passives, such as switchs [14], [15], tunable capacitors [16], [17], inductors [13], [14], transformers [18], [19], and transmission-line and phase shifters [19], [20]. Although all of these RF passives demonstrated high performance, they are standalone off-chip components and have not been integrated with active circuit devices such as a monolithic RF module without a substrate etch [21]. Here, we have successfully integrated MEMS inductors on the top of the CMOS active circuits by employing low-temperature post-CMOS processes. To the best of our knowledge, we are the first to construct a fully integrated VCO with air-suspended MEMS inductors. In this paper, we report design issues, fabrication, and measured performance of the integrated VCO with MEMS inductors in the following sections.

Manuscript received April 24, 2002. This work was supported in part by the Ministry of Science and Technology under the Frontier 21 Program and by the Ministry of Education and Human Resource Development, Korea, under the BK 21 Program.

The authors are with the Division of Electrical Engineering, Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: ecpark@iml.kaist.ac.kr).

Digital Object Identifier 10.1109/TMTT.2002.806510

II. Phase Noise

Phase noise is an important performance measure of VCOs and indicates how pure the signal that the VCO generates is in the frequency domain. For an ideal oscillator, the shape of the spectrum is an impulse at a resonant frequency ω_0. However, in actual oscillators, skirt shape is formed around ω_0. Information recovery from RF signals is seriously affected by this phase noise of VCOs in RF systems [1]. Phase noise can be expressed as signal-to-noise power ratio in unit bandwidth at an offset of $\Delta\omega$ from an oscillation frequency. A simple equation for the phase noise can be written by [22]

$$\mathrm{PN} = 10\log\left\{\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \quad (1)$$

where F is the empirical parameter, k is the Boltzmann constant, T is the absolute temperature, P_s is the signal power, ω_0 is the oscillation frequency, Q_L is the loaded Q of an LC tank, $\Delta\omega$ is the offset frequency, and $\Delta\omega_{1/f^3}$ is the corner frequency at which the slope of phase noise changes from -30 to -20 dB/dec.

A. General Considerations

There are two noise sources that contribute phase noise: thermal noise and flicker noise. Phase noise decreases at 20 dB/dec with respect to offset frequency by the effect of thermal noise, while it decreases at 30 dB/dec by flicker noise. Flicker-noise upconversion is related with the symmetry of a signal waveform and can be reduced by designing VCO signal swings symmetrically [4]. It has been reported that the effect of flicker noise in CMOS transistors can be confined to below 100 kHz, although flicker noise itself in CMOS devices exists over 1 MHz. Thermal noise is proportional to the transconductance of active devices. Active devices in the oscillator generate negative conductance to compensate for the loss in a passive LC tank. If the conductance is too small, it stops VCOs from oscillation. If the conductance is too large, it generates excess thermal noise that may increase phase noise. Therefore, transconductance should be optimized in order to sustain oscillation in a sufficient signal amplitude without introducing excessive noise.

Another important issue is quality factor (Q) of the passive elements in an LC tank of VCOs. It is well known that phase noise decreases inversely proportional to the square of the loaded Q in an LC tank, as shown in (1). When inductors are formed by using standard integrated circuit (IC) processes, the quality factor of inductors is a limiting factor and mainly determines the total Q of an LC tank. Various circuit schemes and their analysis have been reported to improve phase noise by optimizing circuits [3], [4]. However, the fundamental limit in improving phase noise still remains an issue, unless low-quality factors in the LC tank itself can be significantly improved.

B. Transconductance and Phase Noise

Thermal noise becomes a more dominant factor in phase noise than flicker noise in recent RF VCOs. It is because wider channel bandwidth is required as data transfer rates become higher in new RF communication systems. This implies that phase noise of VCOs at higher offset frequencies becomes more important. Typically, system phase-noise requirement is specified at higher frequencies than the corner frequency of VCOs. Therefore, thermal noise becomes a dominant factor that determines phase noise.

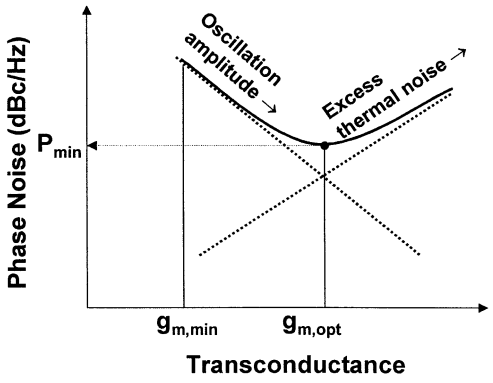

Fig. 1. Transconductance effect on phase noise.

As explained in the previous section, transconductance can be optimized in a given VCO. Fig. 1 shows the transconductance effect on phase noise. The VCO starts oscillating when transconductance reaches to the point $g_{m,\min}$ and it barely compensates for the dissipation in a passive LC tank. After this point, phase noise decreases as transconductance increases because oscillation amplitude becomes larger. However, there is a counter effect. Thermal noise in active CMOS devices increases as transconductance and tail current become larger. Therefore, phase noise reaches the minimum at the point that the signal amplitude effect is completely nullified by thermal noise increase. After passing the minimum point, phase noise increases as the signal amplitude is limited to the supply voltage, while thermal noise continuously increases with the increase of transconductance. Therefore, at any given VCO circuit schemes, there exists an optimum transconductance for the minimum phase noise.

C. Quality-Factor Effects

Fundamentally, phase noise is limited by the quality factor of an LC tank, although the VCO circuit can be designed to give symmetric signal swings and transconductance can be optimized for a given thermal noise. Fig. 2 shows the quality-factor effect on phase noise. Phase noise decreases as Q increases at a fixed transconductance due to a noise-sharpening effect. As the Q of an LC tank increases, the spectrum of the oscillator is sharpened and the noise injected by active devices decreases. Further phase-noise reduction can be achieved by adjustment of transconductance. The optimal transconductances exist at different points with respect to various Q's. VCO circuits with higher Q's require lower transconductance for the minimum phase noise. Lower transconductance can allow lower power dissipation as well. Therefore, the most effective way to improve phase noise in VCOs is to provide high-Q LC resonators. Higher Q of the LC resonator improves phase noise until the Q of the MOS transistor becomes a limiting factor. Typically, the

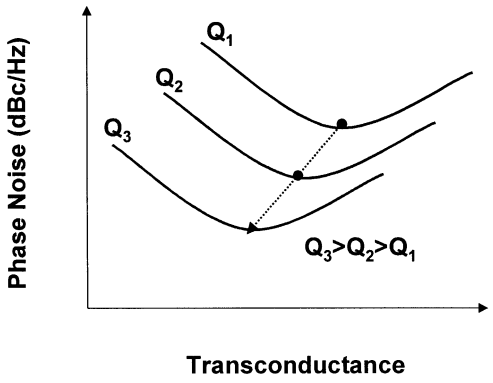

Fig. 2. Quality-factor effect on phase noise.

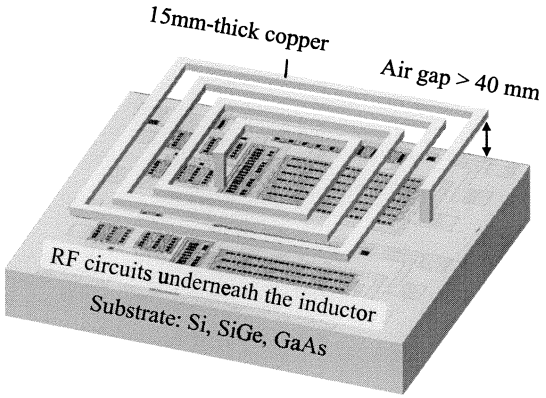

Fig. 3. Conceptual schematic of an integrated VCO with on-chip MEMS inductors.

Q of a MOS transistor is higher than that of CMOS inductors [23].

III. MEMS Inductors

Generally, the inductors obtained from standard silicon processes cannot provide high-Q factors sufficient for high-performance VCOs. The reasons for low-Q factors come from thin metal layers (ohmic loss) and high substrate coupling (eddy-current loss) in standard silicon processes.

Recently, research has been actively carried to find alternative solutions to achieve high-Q inductors from existing silicon processes. Several methods have been proposed to improve Q factors: bond-wire inductors [24], surface acoustic-wave (SAW) resonators with high Q's [25], oxidized porous silicon substrate for thick insulation layer [26], and bulk micromachining for suspended inductor structures [27]. From these methods, high-Q inductors can be achieved, but it is very difficult to monolithically integrate these inductors with on-chip VCO circuits.

We have reported an integrable MEMS fabrication process for RF and microwave MEMS applications [12], [19]. This process allows to fabricate highly suspended metal microstructures that are fully CMOS compatible and manufacturable in terms of process stability and structural robustness. In this section, we will present the RF performance of the suspended spiral inductors fabricated on the standard silicon substrate ($1\sim30\ \Omega\cdot$cm) by using surface micromachining techniques.

A. High-Q MEMS Inductors

In order to implement high-Q inductors on a silicon substrate, two major loss mechanisms to limit Q's in standard CMOS processes have to be minimized. One is ohmic or resistive loss. This loss comes from relatively thin ($0.5\sim2\ \mu$m) metal layers. High resistive loss of these layers plays an important role in determining the Q's at a lower frequency region below a Q peak point. In order to reduce the resistive loss, low-resistivity material should be used as well as the thickness of metal layers should be much larger than skin depth. In this study, we used electroplated thick copper layers, which have a low resistivity of $1.7\ \mu\Omega\cdot$cm and the thickness of 15 μm. The Q's of inductors start to be saturated at the thickness of 10 μm and there is little increment in Q's beyond 15 μm.

The other loss mechanism to be minimized is substrate-induced loss. Integrated passive devices residing on the top of the silicon substrate have electromagnetic coupling to the conductive substrate, resulting in substrate loss [28]. In typical CMOS processes with six metal layers, the top layer metal used for inductors is away from the substrate by no less than 6 μm [11] and electromagnetic energy is coupled and dissipated through the lossy substrate. In addition to that, IC foundry recommends RF designers not to put other circuitry beneath and close ($\sim50\ \mu$m) to CMOS inductors so that the large chip area is consumed by the inductors. This substrate coupling can be significantly reduced by using a suspended metal structure from the substrate. In this study, we built MEMS inductors suspended by 40 μm from the top most layer and could significantly reduce substrate loss.

Fig. 3 shows the conceptual schematic that we have proposed for a single-chip RF transceiver [29]. Active circuit components are fabricated by using standard IC processes and high-performance inductors are monolithically integrated on the top of the circuits by MEMS technology. The features of the proposed MEMS inductors have thick and highly suspended structures for low resistance and low substrate coupling. Due to negligible substrate coupling, MEMS inductors can be stacked on active circuit devices, resulting in the saving of chip area.

B. CMOS-Compatible Integration Process

As a post-CMOS process, special surface micromachining processes have been developed to provide a monolithic solution for high-Q inductors by using conventional lithography and electroplating processes. Basically, thick photoresist lithography frequently used in MEMS applications is employed to form an electroplating mold as well as a sacrificial layer. Copper electroplating then follows to fill the patterned photoresist mold. Finally, photoresist is removed.

Detailed process flows are explained in the following [12]. Fabrication starts with a wafer on which CMOS active devices, as well as metal interconnection lines and a top insulation layer with pad openings have been completed [see Fig. 4(a)]. Ti/Cu (20/100 nm) is thermally evaporated as a seed layer for electroplating. Thick photoresist (AZ9260, approximately 20 μm) is spun and patterned to form electroplating molds. Cu is electroplated through the mold to form bottom electrodes [see Fig. 4(b)]. Second thick photoresist (approximately 40 μm) is spun on the wafer and the two-step UV exposure

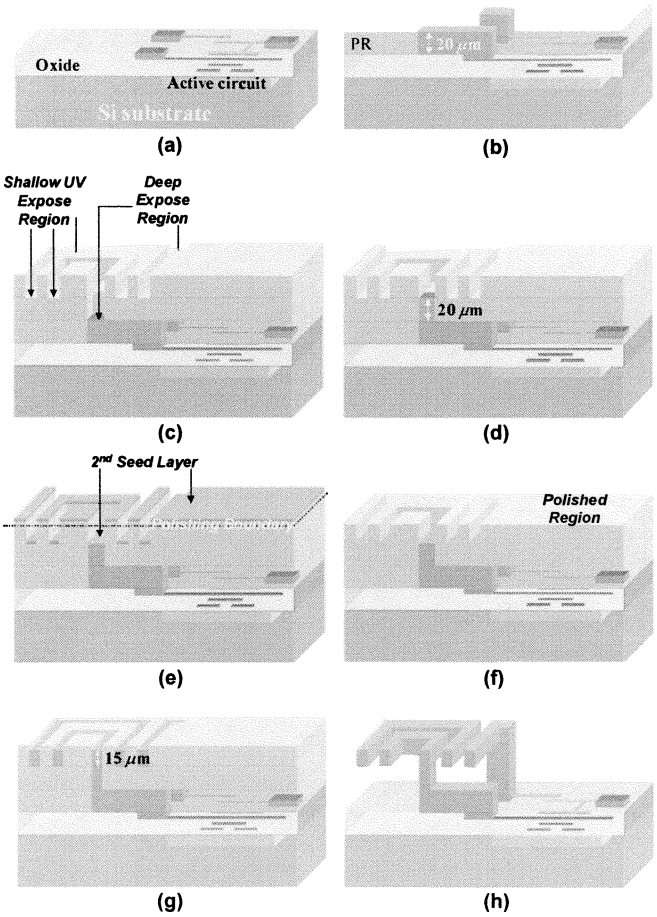

Fig. 4. MEMS inductor integration process.

with two different photomasks and exposure times follows. A three-dimensional (3-D) photoresist mold is formed by single-step development [see Fig. 4(c)]. The thickness of developed photoresist is well controlled by UV expose time [30]. The lower recessed region (approximately 20 μm) is filled with the electroplated Cu to form the posts [see Fig. 4(d)]. After the post electroplating, a second seed metal (Cu) is deposited by thermal evaporation on the wafer [see Fig. 4(e)]. The topmost seed metal is removed in order to confine the electroplating of Cu only in the upper recessed region [see Fig. 4(f)]. The dashed line shown in Fig. 4(e) indicates the boundary to which the mechanical polishing is done. Cu is then electroplated from the bottom of upper recessed region [see Fig. 4(g)]. Finally, suspended MEMS structures are completed by removal of photoresist and seed layers [see Fig. 4(h)].

IV. Design of CMOS VCO

A. CMOS Cross-Coupled VCO

In this study, a cross-coupled VCO scheme has been chosen because it can generate large and symmetric signal swings [4]. A circuit schematic of the implemented VCO is shown in Fig. 5. Oscillation frequency is determined by inductance and capacitance in the LC tank. An accumulation-mode MOSFET varactor known to give a high-Q and a large tuning range has been used for frequency tuning [31]. A MEMS inductor proposed in

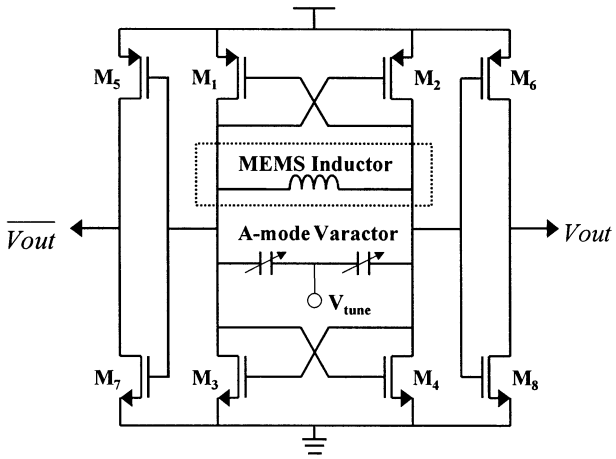

Fig. 5. Circuit schematic of CMOS cross-coupled VCO.

the previous section has been implemented for a high-Q resonator. Adequate transconductance of active devices to compensate for the loss in the passive LC tank is provided by four transistors (M1$\sim$M4). To isolate the LC tank from the 50-Ω termination of the spectrum analyzer, four additional transistors (M5$\sim$M8) have been used as buffer stages. In this scheme, a current source is not employed in order to maximize signal swings and minimize any noise generated from additional active devices. The output signal is measured via a dc blocking capacitor embedded in the circuit. No additional external components have been used for matching.

B. VCO Circuit Optimization

An oscillator is a positive feedback system consisting of an LC resonator and a loss-compensation amplifier. There are two design guidelines to achieve low phase-noise VCOs: one is to maximize the Q of an LC resonator and the other is to minimize the upconversion of noise from the amplifier at a given Q, as described in Section II. Design procedure begins from the optimization of an LC resonator. The total Q of an LC resonator is typically limited by the Q of the inductor. In this study, MEMS inductors have been designed to give a maximum Q at the operating frequencies. We first fixed the width and space of inductors as 30 and 20 μm, respectively. These numbers are determined to achieve a sufficient process margin for inductor fabrication in a reasonable size. The adequate MEMS inductor dimension is then optimized by using 3-D field simulations, which will be confirmed by the measurement of fabricated inductors on a test wafer. The dimensions of the inductors are 220 μm in the inner diameter with 3.25 turns for 1-GHz operation and 220 μm in the inner diameter with 2.25 turns for 2.6-GHz operation, respectively. The target inductances are 5 and 1.8 nH, respectively. The corresponding capacitors in the LC resonators are determined to be 5 and 2 pF for 1- and 2.6-GHz operations, respectively.

To minimize the noise conversion effect, the Agilent ADS simulation tool has been used. The active devices optimization procedure has been proceeded in the following two steps.

Step 1) The ratio of nMOS and pMOS transistors have been optimized for flicker noise reduction.

Step 2) The actual nMOS transistor widths have been determined for thermal noise reduction.

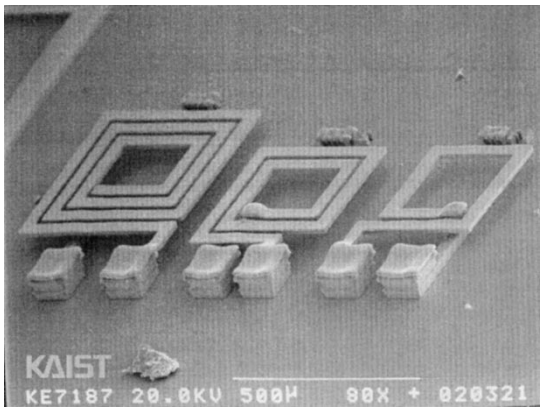

Fig. 6. SEM photograph of fabricated MEMS inductors suspended from the substrate by 40 μm.

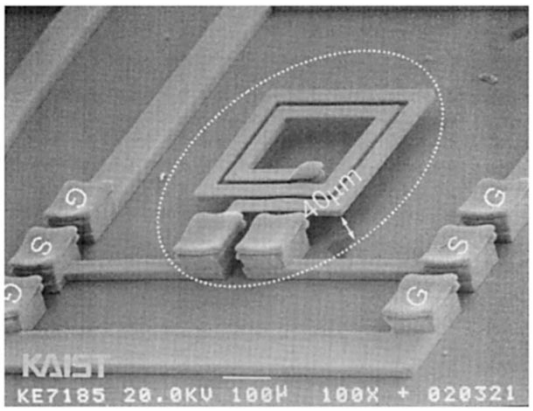

Fig. 7. Measurement pattern to characterize MEMS inductors.

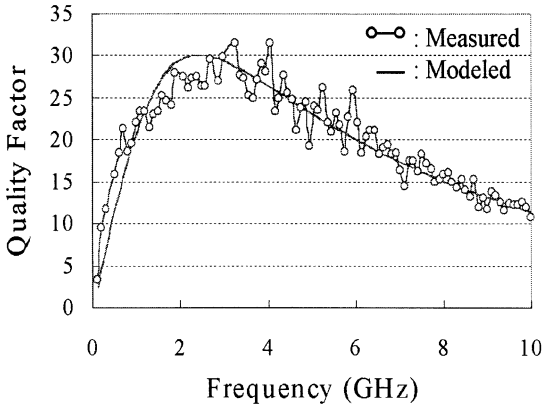

Fig. 8. Measured quality factor of 1.8-nH MEMS inductor.

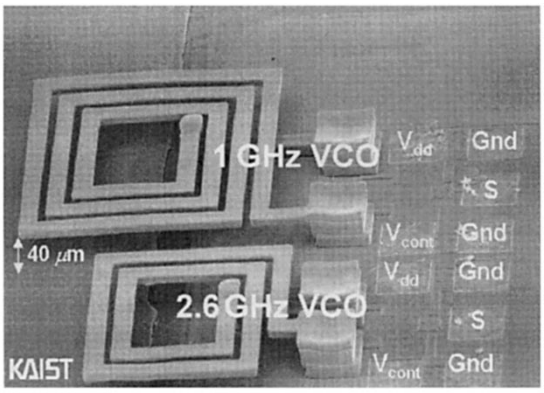

Fig. 9. SEM photograph of fully integrated CMOS VCOs with MEMS inductors.

From simulation results, we have obtained the optimal ratio of nMOS and pMOS transistors as 1 : 2.5, regardless of nMOS size. The result agrees with the inverse ratio of nMOS and pMOS mobilities. This means the optimized VCO will generate a maximum swing of symmetric signals at this ratio. After determining the transistor ratio, the final width of nMOS transistors has been optimized as 16 μm (with 4-μm-width legging) for minimal phase noise at the given Q factor.

V. Experimental Results

A. MEMS Inductor Performance

Fig. 6 shows the fabricated MEMS inductors using surface micromachining technology on a silicon test wafer. The test wafer has 1-μm-thick oxide on the top of the substrate silicon (10 $\Omega\cdot$cm) for electrical isolation. The main body of the MEMS inductors is suspended from the substrate by 40 μm. To characterize the fabricated inductors, on-wafer RF measurement has been performed from 0.1 to 10 GHz using an HP8720 network analyzer. Measurement patterns and deembedding patterns have been fabricated on the same wafer. Fig. 7 shows a measurement pattern of 1.8-nH MEMS inductors. A pad deembedding process has been conducted to exclude parasitic components of the pads incorporated in measurement patterns.

After deembedding, only the intrinsic characteristics of MEMS inductors (inner circle of Fig. 7) can be extracted. The measured and simulated Q's of the fabricated MEMS inductor of 1.8 nH are shown in Fig. 8. Similar characteristics have been obtained from the measurement of 5-nH MEMS inductor. The measured Q's of MEMS inductors are 20 for 5-nH inductors at 1 GHz and 27 for 1.8-nH inductors at 2.6 GHz, respectively. The actual Q's of the integrated MEMS inductors are expected to be higher than these measured values because they will be integrated on the top of the CMOS chip, which may have additional insulation layers (with the total thickness of approximately 6 μm).

B. Phase Noise of Integrated VCO

Monolithic VCOs have been fabricated by integrating MEMS inductors on the top of the active circuits realized using the TSMC 0.18-μm CMOS process. The fabricated VCOs are shown in Fig. 9.

Phase noise has been measured using an HP8564E spectrum analyzer and its characteristics for the 1-GHz oscillator are shown in Fig. 10 as an example. Similar characteristics have been measured for the 2.6-GHz VCO. Low phase noise has been measured as -124 dBc/Hz for the 1-GHz VCO and -117 dBc/Hz for the 2.6-GHz VCO at 300-kHz offset, respectively.

Detailed measurement results are summarized and compared with recently reported results of CMOS VCOs [32]–[37] in Table I. Although excellent low phase noise has been achieved, the fabricated VCO could not fully utilize the high performance of MEMS inductors. Unfortunately, unlike the assumption

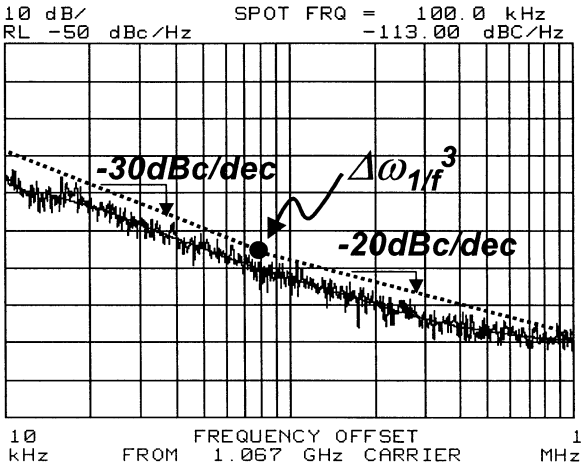

Fig. 10. Measured phase noise of 1-GHz VCO.

TABLE I
MEASURED RESULTS COMPARED WITH OTHER CMOS VCOS

Ref.	Freq. (GHz)	Tuning (MHz)	PN @300kHz (dBc/Hz)	V_{DD} (V)	I_{supply} (mA)	FOM [5]
1GHz (This work)	**1**	**750 (70%)**	**-124**	**3**	**5**	**183**
2.6GHz (This work)	**2.6**	**1600 (61%)**	**-117**	**3**	**5**	**184**
[32] Quad.*	1.8	330 (20%)	-117	2	25	176
[33] Trans.**	1.7	107 (6.3%)	-129	2.5	4.5	193
[34]	1.8	540 (30%)	-116	2.5	4	182
[35] Quad.*	2.45	400 (15%)	-105	1.8	3	174
[36] Quad.*	2.4	300 (14%)	-104	2.5	13	161
[37]	2.5	400 (17%)	-110	3	12	174

*Quad: Quadrature VCO, **Trans: Transformer-based VCO

in the design, the actual varactor Q has been measured as approximately ten at the operating frequencies. There has been some phase-noise degradation compared with simulation. This is because the fabricated varactor has been designed to give an excessive wide tuning range. At least 5-dB improvement can be expected in phase noise, if the varactor Q were to be 20, as assumed. The Q of varactors is inversely proportional to its capacitance value at a given frequency. This means a smaller varactor has a higher Q. Therefore, a higher Q can be achieved by combining a smaller varactor and a high-Q fixed capacitor in parallel at a cost of reduced the tuning range. From phase-noise data shown in Fig. 10, it can be noted that the corner frequency exists below 100 kHz. This indicates that the fabricated VCO has been fully optimized for reducing flicker noise. The VCO tuning range has been measured by varying the control voltage of the varactor from 0 to 4 V. The oscillation frequency has been tuned from 1.08 to 1.83 GHz and from 2.6 to 4.2 GHz for the 1- and 2.6-GHz VCOs, respectively. Fig. 11 shows the measured tuning characteristics of the 2.6-GHz VCO. VCOs consume 15 mW in the VCO core from a 3-V power supply.

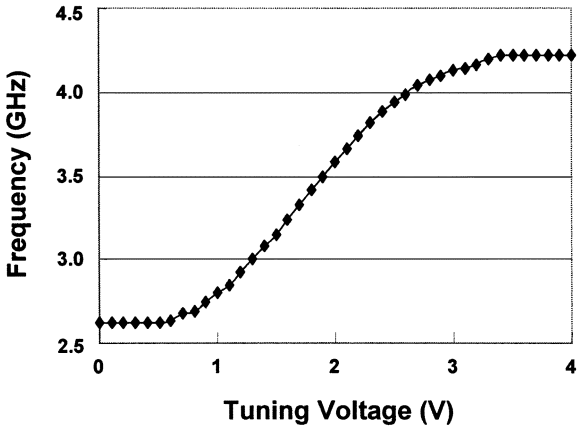

Fig. 11. Tuning characteristics of the 2.6-GHz VCO.

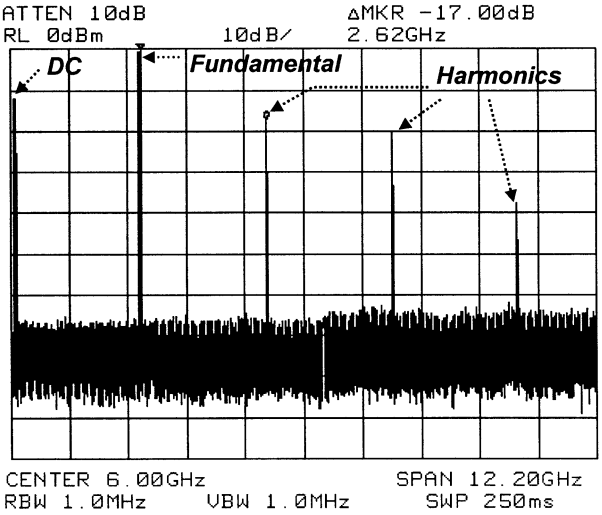

Fig. 12. Output spectrum of the 2.6-GHz VCO.

Fig. 12 shows the output spectrum of the fabricated 2.6-GHz VCO.

VI. CONCLUSIONS

In order to achieve high-performance fully integrated CMOS VCOs, high-Q MEMS inductors have been monolithically integrated on the top of VCO circuit cores. We have achieved high-Q factors over 20 at 1 GHz and 27 at 2.6 GHz, respectively, in the suspended spiral MEMS inductors fabricated using surface micromachining technology. A differential VCO core circuit has been designed and optimized for low phase noise and has been fabricated by the TSMC 0.18-μm CMOS process. From the integrated VCOs with on-chip MEMS inductors, low phase noise has been achieved as -124 dBc/Hz for the 1-GHz VCO and -117 dBc/Hz for the 2.6-GHz VCO at 300-kHz offset from the center frequencies, respectively. We have demonstrated for the first time that the integrated MEMS inductors can give a fully monolithic solution for high-performance on-chip VCOs.

ACKNOWLEDGMENT

This work was performed as part of the National Research Laboratory Program of the Ministry of Science and Technology.

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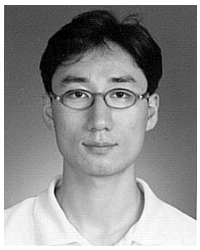
Eun-Chul Park was born in Taegu, Korea. He received the B.S. degree in electronic engineering from the Kyungpook National University, Taegu, Korea, in 1996, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejeon, Korea, in 1998, and is currently working toward the Ph.D. degree at KAIST.

His current interest concerns the integrated MEMS RF module. His current research focuses on high-performance VCOs for RF and microwave applications using MEMS structures.



Yun-Seok Choi was born in Busan, Korea. He received the B.S. degree in electronics engineering from the Busan National University, Busan, Korea, in 1997, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1999, and is currently working toward the Ph.D. degree at KAIST.

His research interests include modeling of RF passive components and 3-D microstructure fabrication technology.

Jun-Bo Yoon (S'92–A'99–M'01) received the B.S. (*summa cum laude*), M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993, 1995, and 1999, respectively. His doctoral research concerned the development of the three-dimensional microstructure technology (3D MEMS) for microfluidic systems and integrated inductors.

From 1999 to 2000, he was with The University of Michigan at Ann Arbor, as a Post-Doctoral Research Fellow, where he demonstrated a movable dielectric tunable micromechanical capacitor for RF applications. In 2000, he returned a Research Assistant Professor to the Department of Electrical Engineering, KAIST, where he is currently an Assistant Professor. His research interests include microfabrication and nanofabrication (3-D microstructure and nanostructure) technologies, micro/nanosensors and actuators, optical MEMS, bio MEMS, and RF/microwave MEMS.

Dr. Yoon was the recipient of the Third-Place Award of the Student Paper Competition presented at the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) in June 1999.

Songcheol Hong (S'87–M'88) was born in Korea, in 1959. He received the B.S. and M.S. degrees in electronics engineering from the Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degrees in electrical engineering and computer science from The University of Michigan at Ann Arbor, in 1989.

He is currently a Professor in the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. He has been interested in monolithic microwave ICs and novel quantum devices. His current research interests include solid-state power amplifiers, large-signal models for microwave device, and quantum dot and well application.

Dr. Hong is a member of KITE.

Euisik Yoon (S'80–M'82) received the B.S. and M.S. degrees in electronics engineering from the Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1990.

From 1990 to 1994, he was with the Fairchild Research Center, National Semiconductor Corporation, Santa Clara, CA, where he was engaged in research on deep-submicrometer CMOS integration and advanced gate dielectrics. From 1994 to 1996, he was a Member of Technical Staff with Silicon Graphics Inc., Mountain View, CA, where he was involved with the design of the MIPS microprocessor R4300I and the RCP 3-D graphic coprocessor. In 1996, he joined the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, where he is currently an Associate Professor. His current research interests are MEMS, integrated microsystems, and very large scale integration (VLSI) circuit design.

Dr. Yoon has served on various Technical Program Committees including the Microprocesses and Nanotechnology Conference, International Sensor Conference, and IEEE Asia–Pacific Conference on Application Specific Integrated Circuits (ASICs). He currently serves on the IEEE International Solid-State Circuits Conference (ISSCC) Program Committee and Transducers Technical Program Committee.