CURRICULUM VITAE

Keshab K. Parhi
Erwin A. Kelen Chair in Electrical Engineering
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Department of Electrical & Computer Engineering (ECE)
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March 15, 2024

EDUCATION

- Ph.D., Electrical Engineering and Computer Sciences, University of California, Berkeley, September 1988, Research Advisor: Prof. David G. Messerschmitt.
  THESIS: Algorithm and Architecture Designs for High-Speed Digital Signal Processing

- M.S.E.E., Univ. of Pennsylvania, Philadelphia, May 1984, Concentrated on signal processing and VLSI IC design. Research Advisor: (Late) Prof. Raymond S. Berkowitz.
  THESIS: Application of Importance Sampling for False Alarm Setting in Complex Multi-Dimensional Signal Processing Systems

- B.Tech. (Honors), Indian Institute of Technology, Kharagpur, India, May, 1982, Electrical Engineering.

INDUSTRIAL AND ACADEMIC EXPERIENCE

- Professor (Tenured), Department of Electrical Engineering, University of Minnesota, Minneapolis, MN, 55455 (starting July 1995). Erwin A.Kelen Chair in Electrical Engineering (July 2022-). Edgar F. Johnson Professor (July 1997-June 2022). Distinguished McKnight University Professor (Starting July 2000). Associate Professor with Tenure (July 1992 - June 1995), Assistant Professor (Oct. 1988 - June 1992)

  Research efforts directed towards VLSI Architectures for Digital Signal Processing, Machine Learning and Artificial Intelligence, Error Control Coders, Cryptography, Hardware Security, and DNA Signal Processing and DNA Machine Learnig. Current research is also directed towards data-driven neuroscience, classification of neurological and psychiatric disorders such as epilepsy, Parkinson's, schizophrenia, and mental disorders such as obsessive compulsive disorder (OCD), borderline personality disorder (BPD) and major depressive disorder (MDD) from MEG, EEG, intra-cranial EEG,

Local Field Potentials, and functional MRI. Other intersts include computational neuroscience, causality in networks of time series, and brain connectivity.

Past research has addressed VLSI Digital Filters, Adaptive Filters and Beamformers, Architectures for Wired and Wireless Communications including Ethernet over Copper and Fiber, Serdes and Backplanes, Video Compression, Computer Arithmetic, Low-Power Digital Systems, CAD for DSP and for Low-Power, High-Level Synthesis, Digital IC Design, and FPGA System Prototyping. Past research also has addressed opthalmic image analysis from fundus images and OCT, and classification of diabetic retinopathy, diabetic macular edema (DME) and age-related macular degeneration (AMD).

- Visiting Professor, Stanford University, 2018
- Visiting Professor, Fudan University, Shanghai, China, 2017
- Director of Graduate Studies of the Electrical Engineering Program, University of Minnesota, July 2008 - September 2011
- President, Leanics Corporation, 2005-2012
- Medtronic, Inc., Minneapolis, MN, 2006-2007, on Sabbatical Leave
- Broadcom Corp., Irvine, (2000-2002), Senior Principal Scientist and Technical Director - DSP Systems, Office of CTO (on Leave)
- Technical Advisory Board, Morphics, Inc. (2002-2003)
- Visiting Professor, Lund Univ., Sweden (April 1999)
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (1996-97 Academic Year, on Leave as National Science Foundation Fellow)
- Visiting Professor, Delft Univ., The Netherlands (March - April, 1996)
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (April 1992 - June 1992), Researched VLSI Architectures for Discrete Wavelet Transforms.
- Consultant to Dorsey and Whitney (2007), Theseus Logic (1996-1999), United Nations Development Program (1995), Top-Vu Technology, Inc. (1994), US West Advanced Technologies (1989), and Bell Labs (1987 - 1988)
- Summer Job at AT&T Bell Laboratories, Holmdel, NJ during Summer 1987.
- Summer job at the IBM T.J. Watson Research Center, Yorktown Heights, NY, during Summer 1986.

AWARDS AND HONORS

- Fellow, IEEE (1996)

  Citation: For contributions to the fields of VLSI digital signal processing architectures, design methodologies and tools.

- Fellow, Association for Computing Machinery (ACM) (2020)

  Citation: For contributions to architectures and design tools for signal processing and networking accelerators.

- Fellow, National Academy of Inventors (NAI) (2020)

  Citation: For his impact in the fields of electrical engineering and electronic communication.

- Fellow, American Institute for Medical & Biological Engineering (AIMBE) (2022)

  Citation: For outstanding contributions to machine learning approaches for neuropsychiatric and ophthalmic disorders, and to synthesis of molecular computing systems.

- Fellow, American Association for Advancement of Science (AAAS) (2017)

  Citation: For contributions to architectures and methodologies for VLSI design of digital signal processing systems and physical layer communication systems that form the backbone of the Internet

- IEEE Kiyo Tomiyasu Technical Field Award (2003)

  Citation: For pioneering contributions to high-speed and low-power digital signal processing architectures for broadband communications systems.

- Mac Van Valkenburg Award, IEEE Circuits and Systems Society (2017)

  Citation: For pioneering contributions to VLSI digital signal processing architectures, design methodologies, and their applications to wired and wireless communications, and service to IEEE Circuits and Systems Society.

- Charles A. Desoer Technical Achievement Award, IEEE Circuits and Systems Society (2012)

  Citation: For contributions to VLSI srchitectures and design methodologies for digital signal processing and communications circuits and systems.

- John Choma Education Award, IEEE Circuits and Systems Society (2021)

  Citation: For contributions to VLSI signal processing education.

- Distinguished Alumnus Award, Indian Institute of Technology, Kharagpur (2013)

- Award for Outstanding Contributions to Postbaccalaureate, Graduate, and Professional Education, University of Minnesota (2013)

- Charles E. Bowers Faculty Teaching Award, College of Science & Engineering, University of Minnesota (2022)
- Frederick Emmons Terman Award from American Society of Engineering Education (2004)
- IEEE Circuits and Systems Society Golden Jubilee Medal (2000)
- National Science Foundation Young Investigator Award (NYI), 1992-1997
- National Science Foundation Research Initiation Award, 1989
- IEEE Trans. VLSI Systems Prize Paper Award (2017)
- IEEE W.R.G. Baker Best Paper Award (2001)
- Darlington Best Paper Award of the IEEE Circuits and Systems Society, 1994
- Guillemin-Cauer Best paper Award of the IEEE Circuits and Systems Society, 1993
- IEEE Signal Processing Society Paper Award, 1991,
- IEEE Browder J. Thompson Memorial Prize paper Award, 1991
- Best (Student) Paper Award at the 2023 IEEE EMBS Neural Engineering Conference (NER) (2023)
- Best Paper Award at the 2017 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2017)
- Best Paper Award at the 2016 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2016)
- Best (Student) Paper Award for the Design and Implementation of Signal Processing Systems (DISPS) Track at the IEEE ICASSP Conference (2015)
- Best (Student) Paper Award at the 6th IEEE Int. Conference on Neural Engineering (2013)
- Best (Third Place Student) Paper Award, 2012 Asilomar Conference on Signals, Systems and Computers (2012)
- Best (Student) Paper Award at the Asilomar Conference on Signals, Systems and Computers (2004)
- ACM Great Lakes Symp. Best Paper Award, 2004
- Best (Student) Paper Award at the IEEE Signal Processing Systems (SiPS) Workshop (1999)
- Best Paper Award at 33rd Design Automation Conference, June 1996

- Distinguished McKnight University Professorship (2000-)
- Judge, IEEE Fellow Selection Committee (1998-2000)
- IEEE Circuits and Systems Society Distinguished Lecturer (1996-1997)(2019-2021)
- McKnight - Land Grant Professorship at the Univ. of Minnesota, 1992 - 1994
- Eliahu Jury Award (for excellence in systems research), 1987, U.C. Berkeley
- Demetri Angelakos Award (for altruistic activities afforded fellow graduate students), 1987, U.C. Berkeley
- IBM Graduate Fellowship, 1987-88
- U.C. Regents Fellowship, 1986-87

Patents

1. R.A. Freking and K.K. Parhi, "Fast and Small Serial Variable Length Encoder with an Optimally High Rate for Encoding Including Huffman Encoding", U.S. Patent Number 6,271,689, August 7, 2001

2. R.A. Freking and K.K. Parhi, "Concurrent Method for Parallel Huffman Compression Coding and Other Variable Length Encoding and Decoding", U.S. Patent Number 6,304,197, October 16, 2001

3. R.A. Freking and K.K. Parhi, "Fast and Small Serial Huffman Decoder for Decoding at an Optimally High Rate", U.S. Patent Number 6,307,489, October 23, 2001

4. W. Freking and K.K. Parhi, "Fast Parallel cascaded Array Modular Multiplier", U.S. Patent Number 6,892,215, Issued May 10, 2005

5. K.K. Parhi, "System and Method for Generating Cyclic Codes for Error Control in Digital Communications", US Patent Number 6,895,545, Issued May 17, 2005

6. W. Freking and K.K. Parhi, "Systolic Cylindrical Array Modular Multiplier", US Patent Numbber 6,907,440, Issued June 14, 2005

7. K.K. Parhi, J.G. Chung, and K.J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier", US Patent Number 6,978,426, Issued December 20, 2005

8. W. Freking and K.K. Parhi, "Systolic Ring Planarized Cylindrical Array Modular Multiplier", US Patent 7,010,561, Issued March 7, 2006

9. K.K. Parhi, "Pipelined Add-Compare-Select Circuits and Methods, and Applications there of", US Patent 7,020,831, Issued March 28, 2006

10. K.K. Parhi, J.-G. Chung and S.-M. Kim, "Low-Error Canonic-Signed-Digit Fixed-Width Multiplier, and Method for Designing Same", US Patent 7,080,115, Issued July 18, 2006

11. T. Zhang and K.K. Parhi, "LDPC Code and Encoder/Decoder Regarding Same", US Patent 7,120,856, Issued Oct. 10, 2006

12. Z. Wang and K.K. Parhi, "Area-Efficient Parallel Turbo Decoding", US Patent 7,200,799, Issued April 3, 2007

13. K.K. Parhi, "Pipelining of Multiplexor Loops in a Digital Circuit", US Patent 7,239,652, Issued July 3, 2007

14. K.K. Parhi and J. Kong, "Low-Latency Architectures for High-Throughput Viterbi Decoders", US Patent 7,308,640, Issued December 11, 2007

15. K.K. Parhi, "Pipelined Parallel Processing of Feedback Loops in a Digital Circuit", US Patent 7,333,580, Issued Feb. 19, 2008

16. K.K. Parhi, J.-G. Chung, K.-C. Lee, K.-J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier," US Patent 7,334,200, Feb. 19, 2008

17. K.K. Parhi, "System and method for generating cyclic codes for error control in digital communications", US Patent 7,539,918, Issued May 26, 2009

18. K.K. Parhi and Y. Gu , "System and Method for MIMO Equalization for DSP Transceivers", US Patent 7,561,633, Issued July 14, 2009

19. A.E. Cohen and K.K. Parhi, "Low-Complexity Hybrid LDPC Code Encoder", US Patent 7,657,816, Issued Feb. 2, 2010

20. Y. Gu and K.K. Parhi, "Parallel Tomlinson Harashima Precoders", US Patent 7,693,233, Issued April 6, 2010

21. S.M. Kim, K.K. Parhi, and R. Liu, "System and Method for Designing RS Based LDPC Code Decoder", US Patent 7716553, Issued May 11, 2010

22. K.K. Parhi and Y. Gu, "High-Speed Precoders for Communications Systems", US Patent 7,769,099, Issued August 3, 2010

23. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", Us Patent 7,933,341, Issued April 26, 2011

24. K.K. Parhi and Y. Gu, "System and Method for Low-Power Echo and NEXT Cancellers", US Patent 8,009,823, Issued August 30, 2011

25. A. Cohen and K.K. Parhi, "System for Secure Variable Data Rate Transmission", US Patent 8,416,948, Issued April 9, 2013

26. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", US Patent 8,422,591, Issued April 16, 2013

27. J. Chen and K.K. Parhi "System for MIMO equalization of multi-channel transceivers with precoding," US Patent 8,498,343, Issued July 30, 2013

28. J. Chen and K.K. Parhi, "System for Low-Complexity Adaptive Echo and NEXT Cancellers", US Patent 8,600,039, Issued Dec. 3, 2013

29. J. Chen and K.K. Parhi, "System for FEXT Cancellation of Multi-Channel Transceivers with Precoding", US Patent 8,699,551, Issued April 15, 2014

30. Y. Lao, K.K. Parhi and C.H. Kim, "Robust Device Authentication," US Patent 10,235,517, Issued March 19, 2019

31. K.K. Parhi and Z. Zhang, "Method and apparatus for prediction and detection of seizure activity," US Patent 10,426,365, October 1, 2019

32. K.K. Parhi and S. Koteshwara, "Dynamic Functional Obfuscation, US Patent 11,061,997, Issued July 13, 2021

33. M. Liu, C. Zhou, K.K. Parhi and C.H. Kim, "Stable Memory Cell Identification for Hardware Security," US Patent 11,309,018, Issued April 19, 2022

34. K.K. Parhi and S.V.S. Avvaru, "Feed-Forward XOR Physical Unclonable Functions," US Patent 11,374,774, Issued June 28, 2022

35. X. Zhang and K.K. Parhi, "Reduced Complexity Modular Polynomial Multiplication for RLWE Cryptosystems," US Patent 11,750,366, Issued September 5, 2023

36. M. Liu, C. Zhou, K.K. Parhi and C.H. Kim, "Stable Memory Cell Identification for Hardware Security," US Patent 11,769,548, Issued September 26, 2023

37. K.K. Parhi, X. Zhang, W. Tan, A. Wang, and Y. Lao, "Low Latency Polynomial Modulo Multiplication over Ring," US Patent Application 17,582,560, Filed: January 24, 2022

38. K.K. Parhi, W. Tan, S.-W. Chiu, A. Wang, and Y. Lao, "PARALLEL POLYNOMIAL MODULAR MULTIPLICATION USING NTT AND INVERSE NTT," US Patent Application 18,500,670, Filed: November 2, 2023

39. K.K. Parhi, W. Tan, and Y. Lao, "FAST POINTWISE MULTIPLICATION IN MATRIX-VECTOR POLYNOMIAL MODULAR MULTIPLICATION," US Patent Application 18,532,443, Filed: December 7, 2023

IEEE 802.3 Standards Presentations

1. K.K. Parhi, C. Lutkemeyer, A. Abnous and M. Hatamian, "Parallel Implementation of the DSP Functions of the PAM-5 10 Gb/s Transceiver", IEEE 802 Plenary meeting, March 2000, http://grouper.ieee.org/groups/802/3/ae/public/mar00/parhi_1_0300.pdf

2. O. Agazzi, V. Gopinathan, K. Parhi, K. Kota, A. Phanse, "DSP Based Equalization for Optical Channels", http://grouper.ieee.org/groups/802/3/ae/public/sep00/agazzi_1_0900.pdf

3. K.K. Parhi and Y. Gu, "Interleaved Trellis Coded Modulation and Decoding", http://grouper.ieee.org/groups/802/3/10GBT/public/jul03/parhi_1_0703.pdf

4. K.K. Parhi and Y. Gu, "Pipelining Tomlinson Harashima Precoders", http://grouper.ieee.org/groups/802/3/an/public/sep04/parhi_1_0904.pdf

Books

1. N.R. Shanbhag, and K.K. Parhi, *Pipelined Adaptive Digital Filters*, Kluwer Academic Publishers, 1994

2. R.I. Hartley, and K.K. Parhi, *Digit-Serial Computation*, Kluwer Academic Publishers, 1995

3. T. Nishitani and K.K. Parhi, ed., *VLSI Signal Processing VIII*, IEEE Press, 1995

4. J.-G. Chung and K.K. Parhi, *Pipelined Lattice and Wave Digital Recursive Filters*, Kluwer Academic Publishers, 1996

5. J. Fortes, C. Mongenet, K. Parhi, and V. Taylor, Ed., *Proceedings 1996 International Conference on Application Specific Systems, Architectures, and Processors*, IEEE Computer Society Press, 1996

6. K.K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, NY 1999

7. K.K. Parhi and T. Nishitani, Ed., *Digital Signal processing for Multimedia Systems*, Marcel Dekker, NY, 1999

Book Chapters

1. K.K. Parhi, "Parallel Processing and Pipelining in Huffman Decoder", (Chapter 12) in *VLSI Implementations for Image Communications*, Series Advances in Image Communications (Edited by Peter Pirsch), **Vol. 2**, Elsevier Science Publisher, Amsterdam, 1993, pp. 365-395

2. K.K. Parhi, "VLSI For Signal Processing: Special Architectures", in *The Electrical Engineering Handbook*, edited by Richard C. Dorf, CRC Press, 1993, pp. 370-384 (Chapter 17, Section 17.1)

3. C.Y. Wang, and K.K. Parhi, "The MARS High-Level DSP Synthesis System", in *VLSI Design Methodologies for Digital Signal Processing Architectures*, edited by M. Bayoumi, pp. 169-205, Kluwer Academic Press, 1994

4. K.K. Parhi, "High-Level Transformations for DSP Synthesis", Chapter 8.1 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 575-587, IEEE Press, 1995

5. N.R. Shanbhag and K.K. Parhi, "Pipelined Adaptive Digital Filters", Chapter 8.2 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 589-601, IEEE Press, 1995

6. C.-Y. Wang and K.K. Parhi, "High-Level DSP Synthesis", Chapter 8.4 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 615-627, IEEE Press, 1995

7. K.K. Parhi and F. Catthoor, "Design of High-Performance DSP Systems", Chapter in *Emerging Technologies: Designing Low-Power Digital Systems*, Edited by R. Cavin and W. Liu, pp. 447-507, IEEE Press (ISCAS-96 Tutorial Book)

8. K.K. Parhi, "Low-Power Digital VLSI Approaches", Chapter in *Circuits and Systems in the Information Age*, Edited by Y. Huang and C. Wei, pp. 3-22, IEEE Press, June 1997 (ISCAS-97 Tutorial Book)

9. K.K. Parhi, "Video Compression", *Chapter 2 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 17-41, Marcel Dekker, New York, 1999

10. T.C. Denk and K.K. Parhi, "Wavelet VLSI Architectures", *Chapter 13 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 329-353, Marcel Dekker, New York, 1999

11. K.J. Raghunath and K.K. Parhi, "Pipelined RLS for VLSI: STAR-RLS Filters", *Chapter 19 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 519-550, Marcel Dekker, New York, 1999

12. H.R. Srinivas and K.K. Parhi, "Division and Square-Root", *Chapter 20 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 551-587, Marcel Dekker, New York, 1999

13. L. Song and K.K. Parhi, "Finite Field Arithmetic Architectures", *Chapter 21 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 589-621, Marcel Dekker, New York, 1999

14. J.H. Satyanarayana and K.K. Parhi, "Power Estimation Approaches", *Chapter 25 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 741-772, Marcel Dekker, New York, 1999

15. J.P. Ma and K.K. Parhi, "On Pipelined Implementations of QRD-RLS Adaptive Filters", *Chapter in QRD-RLS Adaptive Filters*, Edited by J.A. Apolinario, Jr., pp. 269-297, Springer-Verlag, 2009

16. K.K. Parhi and Y. Chen, "Signal Flow Graphs and Data Flow Graphs", *Handbook of Signal Processing Systems*, Vol. 4, Edited by S.S. Bhattacharyya, E.F. Deprettere, R. Leupers and J. Takala, pp. 791-816, Springer-Verlag, 2010

17. H.A. Patil, A.E. Cohen, and K.K. Parhi, "Speaker Identification over Narrowband VoIP Networks", *Chapter 6 in Advances in Forensic Speaker Recognition: Criminal Justice and Counterterrorism*, Edited by A. Neustein and H. Patil, Springer Science+Business Media LLC, 2011, pp. 125-151

18. V. Kulkarni, H. Jiang, E. Kharisov, N. Hovakimyan, M. Riedel, K. Parhi, "Synchronous Sequential Computations with Biomolecular Reactions," *Chapter 14 in Systems and Synthetic Biology Book*, Edited by V. Singh and P. K. Dhar, Springer Verlag, Netherlands, 2015, pp. 255-279

19. S. Roychowdhury, D. Koozekanani, M. Reinsbach and K.K. Parhi, "Automated OCT Segmentation for Images with DME," Chapter 4 in *Medical Image Analysis and Informatics: Computer-aided Diagnosis and Therapy*, edited by P.M. de Azevedo-Marques, A. Mencattini, M. Salmeri, and R. M. Rangayyan, CRC Press, pp. 85-102, 2017

Journal Publications

1. K.K. Parhi and D.G. Messerschmitt, "Concurrent Cellular VLSI Adaptive Filter Architectures", *IEEE Transactions on Circuits and Systems*, **Vol. CAS-34**, No. 10, October 1987, pp. 1141-1151

2. K.K. Parhi and R.S. Berkowitz, "On Optimizing Importance Sampling Simulations", *IEEE Transactions of Circuits and Systems*, **Vol. CAS-34**, No. 12, December 1987, pp. 1558-1563

3. K.K. Parhi, and D.G. Messerschmitt, "Concurrent Architectures for Two-Dimensional Recursive Digital Filtering", *IEEE Trans. on Circuits and Systems*, **Vol. CAS-36(6)**, June 1989, pp. 813-829

4. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part I: Pipelining using Scattered Look-Ahead and Decomposition", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1099-1117

5. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part II: Pipelined Incremental Block Filtering", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1118-1135

6. K.K. Parhi, "Algorithm Transformation Techniques for Concurrent Processors", *Proceedings of the IEEE*, Special Issue on Supercomputer Technology, **Vol. 77(12)**, December 1989, pp. 1879-1895

7. K.K. Parhi, and D.G. Messerschmitt, "Static Rate-Optimal Scheduling of Iterative Data Flow Programs via Optimum Unfolding", *IEEE Trans. on Computers*, **Vol. 40(2)**, February 1991, pp. 178-195

8. K.K. Parhi, "A Systematic Approach for Design of Digit-Serial Signal Processing Architectures", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 4, April 1991, pp. 358-375

9. K.K. Parhi, "Pipelining In Dynamic Programming Architectures", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1442-1450

10. K.K. Parhi, "Finite Word Effects in Pipelined Recursive Filters", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1450-1454

11. K.K. Parhi, "Pipelining in Algorithms with Quantizer Loops", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 7, July 1991, pp. 745-754

12. K.K. Parhi, "Technology for the 90s: VLSI Signal and Image Processing Systems", *IEEE Circuits and Devices Magazine* (special technology forecast issue), **7**(4), July 1991 (invited article), pp. 16-17

13. K.K. Parhi, "Research on VLSI For Digital Video Systems in Japan", *Asian Scientific Information Bulletin of the Office of Naval Research Office*, **16**(4), October - December 1991, pp. 93-98

14. K.K. Parhi, C.Y. Wang, A.P. Brown, "Synthesis of Control Circuits in Folded Pipelined DSP Architectures", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 1, January 1992, pp. 29-43

15. M. Hatamian and K.K. Parhi, "An 85-MHz Fourth-Order Programmable IIR Digital Filter Chip", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 2, February 1992, pp. 175-183

16. H.R. Srinivas, and K.K. Parhi, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", *Journal of VLSI Signal Processing*, **Vol. 4**, No. 2/3, 1992, pp. 177-198

17. H.R. Srinivas, and K.K. Parhi, "A Fast VLSI Adder Architecture", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 5, May 1992, pp. 761-767

18. K.K. Parhi, "High-Speed VLSI Architectures for Huffman and Viterbi Decoders", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 6, June 1992, pp. 385-391

19. K.K. Parhi, "Video Data Format Converters Using Minimum Number of Registers", *IEEE Transactions on Circuits and Systems For Video Technology*, **Vol. 2**, No. 2, June 1992, pp. 255-267

20. K.K. Parhi, "Systematic Synthesis of DSP Data Format Converters using Life-Time Analysis and Forward-Backward Register Allocation", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 7, July 1992, pp. 423-440

21. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Differential Vector Quantizer for Low-Power Speech Coding Applications", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **40**(5), May 1993, pp. 347-349

22. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Lattice Filter Architecture", *IEEE Trans. on Signal Processing*, **41**(5), May 1993, pp. 1925-1939

23. K.J. Raghunath, and K.K. Parhi, "Parallel Adaptive Decision Feedback Equalizers", *IEEE Transactions on Signal Processing*, **41**(5), May 1993, pp. 1956-1961

24. K.K. Parhi, and T. Nishitani, "VLSI Architectures for Discrete Wavelet Transforms", *IEEE Trans. on VLSI Systems*, **1**(2), June 1993, pp. 191-202

25. L.E. Lucke, and K.K. Parhi, "Data-Flow Transformations for Critical Path Time Reduction For High-Level DSP Synthesis", *IEEE Transactions on Computer Aided Design of Integrated Circuits And Systems*, **12**(7), July 1993, pp. 1063-1068

26. N.R. Shanbhag, and K.K. Parhi, "Relaxed Look-Ahead Pipelined LMS Adaptive Filters and Their Application to ADPCM Coder", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 40**(12), December 1993, pp. 753-766

27. K.K. Parhi, F.H. Wu, and K. Ganesan, "Sequential and Parallel Neural Network Vector Quantizers", *IEEE Transactions on Computers*, **43**(1), pp. 104-109, January 1994

28. J.-G. Chung, and K.K. Parhi, "Pipelining of Lattice IIR Digital Filters", *IEEE Transactions on Signal Processing*, **42**(4), pp. 751-761, April 1994

29. L.E. Lucke, and K.K. Parhi, "Parallel Processing Architectures for Rank-Order and Stack Filters", *IEEE Transactions on Signal Processing*, **42**(5), pp. 1178-1189, May 1994

30. N.R. Shanbhag, and K.K. Parhi, "Finite Precision Analysis of the ADPCM Coder", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(5), pp. 364-368, May 1994

31. K.K. Parhi, "Calculation of Minimum Number of Registers in Arbitrary Life Time Chart", *IEEE Circuits and Systems Transactions - Part II: Analog and Digital Signal Processing*, **41**(6), pp. 434-436, June 1994

32. N.R. Shanbhag, and K.K. Parhi, "Corrections to "Finite Precision Analysis of the ADPCM Coder"", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(7), pp. 493, July 1994

33. G.B. Adams III, E.J. Coyle, L. Lin, L.E. Lucke, and K.K. Parhi, "Input Compression and Efficient VLSI Architectures for Rank-Order and Stack Filters", *Signal Processing*, **38**, pp. 441-453, August 1994

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382. K.K. Parhi, "Analysis of Stochastic Logic Circuits in Unipolar, Bipolar and Hybrid Formats," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

383. S. Koteshwara, A. Das and K.K. Parhi, "FPGA Implementation and Comparison of AES-GCM and Deoxys Authenticated Encryption Schemes," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

384. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Hierarchical Functional Obfuscation of Integrated Circuits Using a Mode-Based Approach," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

385. A. Koyily, C. Zhou, C.H. Kim, and K.K. Parhi, "An Entropy Test for Determining Whether a Mux PUF Is Linear or Nonlinear," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

386. C. Zhou, K.K. Parhi, and C.H. Kim, "Secure and Reliable XOR Arbiter PUF Design: An Experimental Study based on 1 Trillion Challenge Response Pair Measurements," *Proc. 2017 Design Automation Conference (DAC)*, Austin, Texas, June 2017

387. M. Liu, C. Zhou, Q. Tang, K.K. Parhi and C.H. Kim, "A Data Remanence based Approach to Generate 100% Stable Keys from an SRAM Physical Unclonable Function," *Proc. of 2017 IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, Taipei, Taiwan, July 2017

388. S.V. Sandeep Avvaru, C. Zhou, C.H. Kim and K.K. Parhi, "Predicting Hard and Soft-Responses and Identifying Stable Challenges of Mux PUFs Using ANN," *Proc. of 2017 IEEE Midwest Symp. on Circuits and Systems*, pp. 934-937, Boston, August 2017

389. A. Rashno, D. Koozekanani and K.K. Parhi, "Detection and Segmentation of Various Types of Fluids with Graph Shortest Path and Deep Learning Approache," *MICCAI Retinal OCT Fluid Challenge (RETOUCH)*, Sept. 2017

390. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Molecular Computation of Complex Markov Chains with Self-Loop State Transitions," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 478-483, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

391. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Functional Encryption of Integrated Circuits by Key-Based Dynamic Hybrid Obfuscation," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 484-488, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

392. S. Koteshwara, A. Das and K.K. Parhi, "Performance Comparison of AES-GCM-SIV and AES-GCM Algorithms for Authenticated Encryption on FPGA Platforms," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 1331-1336, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

393. A. Koyily, S.V.S. Avvaru, C. Zhou, C.H. Kim and K. K. Parhi, "Effect of Aging on Linear and Nonlinear MUX PUFs by Statistical Modeling," *Proc. of 23rd Asia and South Pacific Design Automation Conference*, pp. 76-83, Jeju Island, Korea, Jan. 2018

394. A. Koyily, C. Zhou, C.H. Kim and K.K. Parhi, "Predicting Soft-Response of Mux PUFs via Logistic Regression of Total Delay Difference," *Proc. of 2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018

395. Q. Tang, W.H. Choi, L. Everson, K.K. Parhi and C.H. Kim, "A Physical Unclonable Function Based on Capacitor Mismatch in a Charge-Redistribution SAR-ADC," *Proc. of 2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018

396. S. Koteshwara and K.K. Parhi, "Low-Energy Architectures of Linear Classifiers for IoT Applications using Incremental Precision and Multi-Level Classification," *Proc. 2018 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 291-296, Chicago, May 2018

397. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen and K.K. Parhi, "Classifying Treated vs. Untreated MDD Adolescents from Anatomical Connectivity using Nonlinear SVM," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 1-4, July 2018, Hawaii

398. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen and K.K. Parhi, "Biomarkers for Adolescent MDD from Anatomical Connectivity and Network Topology Using Diffusion MRI," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 1152-1155, July 2018, Hawaii

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400. A. Rashno, D.D. Koozekanani, and K.K. Parhi, "Segmentation of Various Types of Fluids with Graph Shortest Path and Convolutional Neural Network," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 3426-3429, July 2018, Hawaii

401. C. Deng, S. Liao, Y. Xie, K.K. Parhi, X. Qian, and B. Yuan, "PermDNN: Efficient Compressed Deep Neural Network Architecture with Permuted Diagonal Matrices," *Proc. 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 189-202, Fukuoka, Japan, Oct. 20-24, 2018

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403. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen, and K.K. Parhi, "Classifying Adolescent Major Depressive Disorder using Linear SVM with Anatomical Features from Diffusion Weighted Imaging," *Proc. 2018 Asilomar Conference on Signals, Systems and Computers*, pp. 1197-1201, Pacific Grove, CA, Oct. 28-Oct. 31, 2018

404. B. Sen and K.K. Parhi, "Constrained Tensor Decomposition Optimization with Applications to fMRI Data Analysis," *Proc. 2018 Asilomar Conference on Signals, Systems and Computers*, pp. 1923-1928, Pacific Grove, CA, Oct. 28-Oct. 31, 2018

405. S.V.S. Avvaru and K.K. Parhi, "Feed-Forward XOR PUFs: Reliability and Attack-Resistance Analysis," *Proc. 2019 ACM Great Lakes Symposium on VLSI*, Washington, D.C., May 2019

406. N.K. Unnikrishnan, M. Garrido, and K.K. Parhi, "Effect of Finite Word-Length on SQNR, Area and Power for Real-Valued Serial FFT," *Proc. 2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, May 2019

407. X. Liu and K.K. Parhi, "Computing Radial Basis Function Support Vector Machine using DNA via Fractional Coding," *Proc. 2019 ACM/IEEE Design Automation Conference*, Article 143, Las Vegas, June 2019

408. A. Ayling, S.V.S. Avvaru, and K.K. Parhi, "Not All Feed-Forward MUX PUFs Generate Unique Signatures," *Proc. 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 43-48, Miami, July 2019

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411. B. Sen and K.K. Parhi, "Predicting Male vs. Female from Task-fMRI Brain Connectivity," *Proc. of 2019 IEEE Engineering and Medicine in Biology Conference (EMBC)*, pp. 4089-4092, Berlin, July 2019

412. A. Koyily and K.K. Parhi, "Converting Unstable Challenges to Stable in MUX-based Physical Unclonable Functions by Bit-Flipping," *Proc. 2019 Asilomar Conference on Signals, Systems and Computers*, pp. 327-331, Pacific Grove, CA, Nov. 3-6, 2019

413. X. Liu and K.K. Parhi, "Training DNA Perceptrons via Fractional Coding," *Proc. 2019 Asilomar Conference on Signals, Systems and Computers*, pp. 614-618, Pacific Grove, CA, Nov. 3-6, 2019

414. B. Sen and K.K. Parhi, "Predicting Tasks from Task-fMRI Using Blind Source Separation," *Proc. 2019 Asilomar Conference on Signals, Systems and Computers*, pp. 2201-2205, Pacific Grove, CA, Nov. 3-6, 2019

415. Q. Zhang, Y. Chen, X. Zeng, K.K. Parhi, and B. Nikolic, "A 3.01 mm^2 65.38Gbs Stochastic LDPC Decoder for IEEE 802.3an in 65 nm," *Proc. IEEE Asian Solid-State Circuits Conference*, pp. 271-274, Macau, China, Nov. 4-6, 2019

416. V. Govindan, S. Koteshwara, A. Das, K.K. Parhi and R.S. Chakraborty, "ProTro: A Probabilistic Counter based Hardware Trojan Attack on FPGA based MACSec enabled Ethernet Switch," *Proc. International Conference on Security, Privacy and Applied Cryptographic Engineering (SPACE)*, pp. 159-175, Gandhinagar, India, Dec. 2019

417. N.K. Unnikrishnan and K.K. Parhi, "An Interleaved Scheduler for Energy-Efficient Backpropagation for Training Neural Networks," *Proc. IEEE Int. Symposium on Circuits and Systems*, Seville, Spain, Oct. 2020

418. L. Ge and K.K. Parhi, "Molecular Physical Unclonable Functions," *Proc. 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 476-481 July 2020

419. X. Zhang and K.K. Parhi, "Reduced Complexity Modular Polynomial Multiplication for R-LWE Cryptosystems," *Proc. of 2021 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 7853-7857, June 2021

420. L. Ge and K.K. Parhi, "Seizure Detection using Power Spectral Density via Hyperdimensional Computing," *Proc. of 2021 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 7858-7862, June 2021

421. S. Sanjeet, B. Sahoo, and K.K. Parhi, "Comparison of Real-Valued FFT Architectures for Low-Throughput Applications Using FPGA," *Proc. 2021 IEEE International Midwest Symposium on Circuits and Systems*, August 2021, pp. 112-115

422. Z. Huai, K.K. Parhi, and X. Zhang, "Efficient Architecture for Long Integer Modular Multiplication over Solinas Prime," *Proc. 2021 IEEE Signal Processing Systems Workshop (SiPS)*, pp. 146-151, Oct. 19-21, 2021

423. R. Billmeyer and K.K. Parhi, "Biological Gender Classification from fMRI via Hyperdimensional Computing," *Proc. 2021 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, pp. 578-582, Oct. 31-Nov. 3, 2021

424. S. Avvaru, N. Provenza, A. Widge and K.K. Parhi, " Decoding Human Cognitive Control Using Functional Connectivity of Local Field Potentials," *Proc. 43rd IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 451-454, Oct. 31 - Nov. 4, 2021

425. S. Avvaru, N. Provenza, A. Widge and K.K. Parhi, "Spectral Features Based Decoding of Task Engagement: The Role of Theta and High Gamma Bands in Cognitive Control," *Proc. 43rd IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6062-6065, Oct. 31 - Nov. 4, 2021

426. S.S. Balaji, B. Sen and K.K. Parhi, "Effect of Modulating fMRI Time-Series on Fluid Ability and Fluid Intelligence for Healthy Humans," *Proc. 43rd IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6070-6073, Oct. 31 - Nov. 4, 2021

427. R. Chen and K.K. Parhi, "Seizure Prediction using Convolutional Neural Networks and Sequence Transformer Networks," *Proc. 43rd IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6483-6486, Oct. 31 - Nov. 4, 2021

428. N.K. Unnikrishnan and K.K. Parhi, "LayerPipe: Accelerating Deep Neural Network Training by Intra-Layer and Inter-Layer Gradient Pipelining and Multiprocessor Scheduling," *Proc. IEEE/ACM Conf. Computer Aided Design (ICCAD)*, Nov. 1-5, 2021

429. W. Tan, A. Wang, Y. Lao, X. Zhang and K.K. Parhi, "Pipelined High-throughput NTT Architecture for Lattice-based Cryptography," *Proc. of Asian Hardware Oriented Security and Trust Symposium (AsianHOST)*, Shanghai, China, Dec. 16-18, 2021

430. N.K. Unnikrishnan and K.K. Parhi, "Multi-Channel FFT Architectures Designed via Folding and Interleaving," *Proc. 2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 142-146, Austin, Texas, May 2022

431. S. Avvaru and K.K. Parhi, "Betweenness Centrality in Resting-State Functional Networks Distinguishes Parkinsons Disease," *Proc. 44th IEEE Engineering in Medicine and Biology Society Conference (EMBC),* pp. 4866-4869, Glasgow, Scotland, July 2022

432. A. Wang, W. Tan, Y. Lao and K.K. Parhi, "Integral Sampler and Polynomial Multiplication Architecture for Lattice-based Cryptography," *Proc. 35th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Austin, TX, Oct. 2022

433. B. Ung, L. Ge and K.K. Parhi, "Premature Ventricular Contraction Beat Classification via Hyperdimensional Computing," *Proc. 2022 Asilomar Conference on Signals, Systems and Computers*, pp. 1306-1310, Pacific Grove, CA, Nov. 2022

434. S.S. Balaji, S.V. Sandeep Avvaru and K.K. Parhi, "Classification of Pretrial vs. Encoding stage for Working Memory Task among Subjects with pFC Lesions and Healthy Controls using Directed Information," *Proc. 2022 Asilomar Conference on Signals, Systems and Computers*, pp. 1310-1315, Pacific Grove, CA, Nov. 2022

435. S.S. Balaji and K.K. Parhi, "Classifying Subjects with PFC Lesions from Healthy Controls during Working Memory Encoding via Graph Convolutional Networks," *Proc. of the 2023 IEEE EMBS Conference on Neural Engineering (NER)*, Baltimore, Maryland, April 25-27, 2023

436. S.S. Balaji and K.K. Parhi, "Classifying Patients with pFC Lesions from Healthy Controls using Directed Information based Effective Brain Connectivity Measured from the Encoding Phase of Working Memory Task," *Proc. of the 2023 IEEE Internation Symposium on Biomedical Imaging (ISBI)*, Cartagena de Indias, Colombia, April 2023

437. S. Sanjeet, R.K. Meena, B. Sahoo, K.K. Parhi and M. Fujita, "IIR Filter-Based Spiking Neural Network," *Proc. 2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterrey, CA, May 2023

438. C. Anderson, X. Liu, and K.K. Parhi, "Analysis of Molecular MUX PUFs with Stochastic Challenges," *Proc. IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*," pp. 40-44, Phoenix, August 2023

439. L. Ge and K.K. Parhi, "Applicability of Hyperdimensional Computing for Seizure Prediction Using LBP and PSD Features from IEEG," *Proc. IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*," pp. 1065-1069, Phoenix, August 2023

440. L. Ge, A. Payani, H. Latapie, and K.K. Parhi, "Classifying Functional Brain Graphs using Graph Hypervector Representation," *Proc. of the 57th Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, Oct. 29-Nov. 1, 2023

441. W. Tan, Y. Lao and K.K. Parhi, "KyberMat: Efficient Hardware Accelerator for Matrix-Vector Multiplication in CRYSTALS-Kyber Scheme via NTT and Polyphase Decomposition," *Proc. of the 2023 IEEE/ACM International Conf. on Computer Aided Design (ICCAD)*, San Francisco, Oct. 31-Nov. 2, 2023

442. K.K. Parhi, "A Low-Latency FFT-IFFT Cascade Architecture," *Proc. of 2024 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, Seoul, April 2024

443. W. Tan, Y. Lao, and K.K. Parhi, "Area-Efficient Matrix-Vector Polynomial Multiplication Architecture for ML-KEM Using Interleaving and Folding Transformation," *Proc. of 2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, May 2024

Conference Abstracts Without Proceedings

1. A. Shea, B. Fett, M. Riedel, and K.K. Parhi, "Synthesizing Sequential Register-Based Computation with Biochemistry," *Proc. of IEEE/ACM International Workshop on Logic Synthesis*, 2009

2. H. Jiang, M. Riedel, and K. Parhi, "Signal Processing Functions with Biomolecular Reactions," *International Workshop on Bio-Design Automation*, Anaheim, CA, 2010

3. H. Jiang, M. Riedel, and K. Parhi, "Iterative Computation with Biomolecular Reactions," *Annual Institute of Biological Engineering Conference*, Boston, MA, 2010

4. H. Jiang, M. Riedel, and K. Parhi, "Digital Signal processing with DNA," *International Conference on DNA Computing*, Pasadena, CA, 2011

5. H. Jiang, M. Riedel, and K. Parhi, "Asynchronous Sequential Computation with Molecular Reactions," *International Workshop on Bio-Design Automation*, San Diego, CA, 2011

6. S. Roychowdhury, K.K. Parhi, M.G. Lawrence, and D.D. Koozekanani, "Automated Screening System for Detecting Diabetic Retinopathy: A Classification Approach," Poster presented at 2012 *Association for Research in Vision and Opthalmology (ARVO) annual meeting*, Fort Lauderdale, May 2012

7. S. Radwan, S. Roychowdhury, J. Tokarev, H.F. Roemhild, K.K. Parhi, and D.D. Koozekanani, "Optical Coherence Tomography Predictors of Visual Outcome in Macular Edema," Poster presented at 2013 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Seattle, May 2013

8. S. Roychowdhury, D.D. Koozekanani, S. Radwan, and K.K. Parhi, "Automated Detection and Location Analysis of Diabetic Cysts in Retinal OCT Images: An Iterative Filtering Approach," Poster presented at 2013 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Fort Lauderdale, May 2013

9. K.K. Parhi and Z. Zhang, "Seizure Prediction using Ratio of Spectral Power from Single EEG Electrode," *Proc. of 6th International Workshop on Seizure Prediction (IWSP6)*, p. 39, Nov. 2013, San Diego

10. S. Roychowdhury, K.K. Parhi, M. Reinsbach, and D.D. Koozekanani, "Automated Intra-Retinal Layer Thickness Profile Analysis in Optical Coherence Tomography Images by Iterative High-Pass Filtering," Poster presented at 2014 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Orlando, FL, May 2014

11. Y. Wang, B. Yuan, K.K. Parhi and R. Victora, "Two-Dimensional Magnetic Recording using a Rotated Head Array and LDPC Code Decoding," *2014 IEEE International Magnetics Conference (INTERMAG) Digest*, Dresden, Germany, May 2014

12. S. Chu, C. Lenglet and K.K. Parhi, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at 2014 *IEEE EMBS BRAIN Grand Challenges Conference*, Nov. 2014, Washington, D.C.

13. K.K. Parhi, "Simple Features and Simple Classifiers for Cyber-Physical Systems: Applications to Seizure Detection and Prediction," Talk presented at *Workshop on Big Data Analytics in CPS: Enabling the Move from IoT to Real-Time Control*, April 2015, Seattle, Washington

14. S. Chu, K.K. Parhi and C. Lenglet, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at the *24th Annual Meeting of the International Society for Magnetic Resonance in Medicine (ISMRM)*, May 30-June 5, 2015, Toronto, Canada

15. Z. Zhang and K.K. Parhi, "Seizure Prediction using Polynomial Support Vector Machine Classification," Poster presented at the 7th *International Workshop on Seizure Prediction*, August 3-6, 2015, Melbourne, Australia

16. S.A. Salehi, K.K. Parhi and M.D. Riedel, "Markov Chain Computations using Molecular Reactions," Poster Presented at the 21st *International Conference on DNA Computing and Molecular Programming (DNA21)*, August 17-21, 2015, Cambridge, MA

17. Y. Wang, B. Yuan, K.K. Parhi, and B. Kumar, "Increased Data Throughput and BER Performance with Rotated Head Array in the Two Dimensional Magnetic Recording," *2016 joint MMM-IEEE International Magnetics Conference (INTERMAG)*, San Diego, Jan. 2016

18. K.K. Parhi, "Network Analysis of Functional Brain Connectivity in Borderline Personality Disorder Using Resting-State fMRI," *2016 Information Theory and Applications (ITA)*, San Diego, Jan. 2016 *(Invited Talk)*

19. A. Rashno, K.K. Parhi, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Intra-Retinal, Sub-Retinal and Sub-RPE Cyst Regions Segmentation in Age-Related Macular Degenration (AMD) Subjects," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

20. J. Kohler, A. Rashno, K.K. Parhi, P. Drayna, S. Radwan, and D.D. Koozekanani, "Correlation Between Initial Vision and Vision Improvement with Automatically Calculated Retinal Cyst Volume in Treated DME after Resolution," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

21. K.K. Parhi, A. Rashno, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Fluid/Cyst Segmentation: A Quantitative Assessment of Diabetic Macular Edema," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

22. S. Chu, B. Klimes-Dougan, K.K. Parhi, M.W. Schreiner, K. Cullen, "Brain Connectivity Correlates with Antidepressant Treatment Response in Adolescents with Major Depressive Disorder," *Society for Research on Adolescence (SRA) Biennial Meeting*, Minneapolis, April 2018

23. N.K. Unnikrishnan and K.K. Parhi, "Memory Access and Latency Reduction in Backpropagation using Systolic Arrays and Gradient Computation Interleaving," *ACM Design Automation Conference*, July 2020

University Sponsored Research Grants

1. "Dedicated VLSI DSPs", *Graduate School Grant-in-Aid*, $33.6k (Sept. 1988 - June 1990)

2. "Equipment for VLSI and Image Processing Laboratory", *Graduate School Grant-in-Aid*, $22.5k (Sept. 1990 - June 1991)

3. "McKnight Land Grant Professorship", *Graduate School*, $39.2k, (July 1992 - June 1994)

4. "Edgar F. Johnson Professorship", *College of Science and Engineering*, $15K per year (July 1997 - present)

5. "Distinguished McKnight University Professorship", *Univ. of Minnesota*, $100k research support, Permanent University title, July 2000

6. "Seizure Prediction Classifier Algorithms and Architectures", IEM, $50K (Jan. 1, 2010 - Jan. 31, 2011) (Co-PI: T. Netoff)

7. "Automated Screening System for Diabetic Retinopathy using Fundus Images", Grant-in-Aid, Graduate School, $31,153, Jan. 1, 2011 - June 30, 2012

8. K.K. Parhi, "Redesigning Signal Processing Education, OIT Faculty Fellowship," $10k (2012-2013)

9. K.K. Parhi, "Graduate/Professional Teaching Award," $15k (2013)

10. K.K. Parhi, D. Koozekanani, "Automated Screening for Hypertensive Retinopathy and Stroke from Fundus Images," IEM, $25k, Jan. 2014-Jan. 2015

Externally Funded Research Grants

1. "VLSI Architecture Designs for High-Speed Signal and Image Processing", **National Science Foundation**, Research Initiation Award, $70k (June 1989 - Jan. 1992)

2. "CAD of Real-Time DSP ICs", **Texas Instruments**, $42k, (July 1989 - June 1992)

3. "Vector Quantizers using Neural Networks", **US West Advanced Technologies**, $8k (Aug. 1989)

4. "Concurrent Architectures for VLSI Signal and Image Processing", **Army Research Office**, $233.6k (March 1990 - Feb. 1993)

5. "Design of Dedicated and Programmable VLSI DSP Systems", **Office of Naval Research**, $425k, (Oct. 1990 - Sept. 1993)

6. "CISE Research Instrumentation", **National Science Foundation**, $76k, (Jan. 1992 - Dec. 1992) (with R. Harjani and G. Sobelman)

7. "NYI: Dedicated VLSI Digital Signal and Image Processors", **National Science Foundation**, NSF Young Investigator Award, $312.5k, (Sept. 1992 - March 1998)

8. "Video Compression using Neural Networks", **Data Card Corporation**, $10k, (Sept. 1992 - June 1993)

9. "Design of Dedicated and Programmable VLSI DSP Systems", **Office of Naval Research**, $403k, (Oct. 1993 - Sept. 1996)

10. "Design of High-Speed Digital Signal Processing Architectures", **Office of Naval Research**, $85k (Sept. 1993 - Aug. 1996)

11. "VLSI System Design Methodologies", **NEC Corporation**, $58k, (May 1993 - June 1999)

12. "Design of High-Speed and Low-Power DSP Architectures", **Army Research Office**, $96k (Sept. 1993 - Aug. 1996)

13. "Design Tools and Architectures for Dedicated DSP Processors", **DARPA/Air Force - RASSP Program**, $600k (Aug. 1993 - Aug. 1996)

14. "Concurrent Architectures for VLSI Signal and Image Processing", **Army Research Office**, $169.5k, (Oct. 1994 - Sept. 1997)

15. "Low-Energy Embedded DSP Systems", **Lucent Technologies, Bell Labs.**, $25k (Oct. 1995 - Sept. 1996)

16. "NSF-CGP Fellowship: VLSI Digital Signal Processing and Multimedia Systems", **National Science Foundation**, $104.8k, (Sept. 1996 - July 1997)

17. "Design of Low-Power Arithmetic Systems", **Office of Naval Research**, $102.7k (Sept. 1996 - Sept. 1999)

18. "Application-Specific DSP System design", **Kawasaki Steel - LSI Division**, $60k, (Aug. 1997 - Aug. 1999)

19. "Programmable and Configurable Digit-Serial Digital Signal Processors", **DARPA/ITO Emedded Systems Program/ACS Program**, $1,454k, (Aug. 1996 - Aug. 2000)

20. "Low-Power Architectures for Video Compression", **Army Research Office**, $108.4k (March 1998 - March 2001)

21. "VLSI Architectures for Wavelets and Finite Field Arithmetic", **Army Research Office**, $305k, (June 1998 - June 2001)

22. "Low-Energy Datapath Design for Programmable Digital Signal Processors", **National Science Foundation**, $321k, (Nov. 2000 - Oct. 2003)

23. "High-Speed and Low-Power Error Control Coders", **Army Research Office**, $366k, (August 2001 - August 2004)

24. "Student Travel Grants for SIPS-2002 Workshop", **National Science Foundation**, $5k, (July 2002 - June 2003)

25. "SIPS-2002 Workshop", **Broadcom Corporation**, $5k, (July 2002 - June 2003)

26. "Student Travel Grants for SIPS-2002 Workshop", **Army Research Office**, $5.4k, (July 2002 - June 2003)

27. "Architecture Design Methodologies for Embedded Systems Terminals", **National Science Foundation**, $150k, (June 2003 - Sept. 2004)

28. "LDPC Decoders", **Chonbuk National University, Korea**, $25k (Jan - Dec. 2004)

29. "Architectures for soft-Decision Reed-Solomon Coders", **Army Research Office**, $250k, (July 2004-June 2007)

30. "Design of High-Speed Transceivers for Ethernet over Copper", **National Science Foundation**, $250k, (August 2004-August 2007)

31. "SBIR Phase I: Design of a 10-Gigabit Ethernet Transceiver Over Copper," **National Science Foundation**, $100k, Grant to Leanics Corporation, (Jan. 2005 - Dec. 2005) (PI: Y. Gu)

32. "Phase-I: Tactical Secure Voice/Variable Data Rate Inter Working Function," **U.S. Navy**, $100k, SBIR Contract to Leanics Corporation (2006-2007) (PI: A. Cohen)

33. "Phase-II: Tactical Secure Voice/Variable Data Rate Inter Working Function," **U.S. Navy**, $750k, SBIR Contract to Leanics Corporation, (2008-2010) (PI: A. Cohen)

34. "Collaborative Research: CPA-DA: Noise-Aware VLSI Signal Processing: A New Paradigm for Signal Processing Integrated Circuit Design in Nanoscale Era", **National Science Foundation**, $150k, (Sept 2008-August 2011)

35. "EAGER: Synthesizing Signal Processing Functions with Biochemical Reactions", **National Science Foundation**, $200k (Sept. 2009-Aug. 2011) (Co-PI: M. Riedel)

36. "SBIR Phase I: High-Rate Low-Power Wireless Telemetry System for Medical Applications," **National Science Foundation**, $100k, Grant to Leanics Corporation, (Jan. 2010 - Dec 2010) (PI: J. Lin)

37. "Phase-I: LeanTec: Field Programmable Gate Array (FPGA) Physical Unclonable Functions," $100k, **U.S. Army**, Contract to Leanics Corporation (Jan. 2011 - Dec. 2011) (PI: A. Cohen)

38. "SHF:Small:Digital Signal Processing with Biomolecular Reactions", **National Science Foundation**, $400k (July 2011-June 2014) (Co-PI: M. Riedel)

39. K. Parhi is a Co-I on the $3M NSF IGERT training grant (PI: Bin He) (2011-2016)

40. Broadcom Foundation Gift, $25k (2012-2013)

41. "Stochastic Computing using Digital Signal Processing," **National Science Foundation**, $375k (Sept. 2013-Aug. 2016)

42. Broadcom Foundation Gift, $25k (2013-2014)

43. Broadcom Foundation Gift, $25k (2014-2015)

44. "SHF:Small:Advanced Digital Signal Processing with DNA", **National Science Foundation**, $400k (August 2014-July 2017) (Co-PI: M. Riedel)

45. "Design of Secure and Anti-Counterfeit Integrated Circuits", **Semiconductor Research Corporation**, $168k (Oct. 2014-Sept. 2017) (Joint with NSF) (Co-PI: C. Kim)

46. "Design of Secure and Anti-Counterfeit Integrated Circuits", **National Science Foundation**, $332k (Oct. 2014-Sept. 2018) (Co-PI: C. Kim)

47. "EAGER: Low-Energy Architectures for Machine Learning," National Science Foundation, $125k (Aug. 2017-Aug. 2018)

48. "SHF: Small: Collaborative Research: LDPD-Net: A Framework for Accelerated Architectures for Low-Density Permuted-Diagonal Deep Neural Networks," National Science Foundation, $291k,(Oct. 2018-Sept. 2022)

49. "Collaborative Research: SHF: Medium: TensorNN: An Algorithm and Hardware Co-design Framework for On-device Deep Neural Network Learning using Low-rank Tensors," National Science Foundation, $400k,(July 2020-June. 2023)

50. "Efficient Hardware Accelerator for Fully Homomophic Encryption," **Semiconductor Research Corporation**, $137k (Oct. 2020-Sept. 2023)

51. "Physical Unclonable Function using DNA," **Army Research Office**, $150k, (May 2021-Jan. 2024)

52. "Hyperdimensional Computing Classifiers for Low-Energy Edge Computing," **CISCO**, $125k, (Sept. 2021 - Aug. 2022)

53. "Hyperdimensional Computing for Embedded Graphs," **CISCO**, $140k (October 2022 - Sept. 2023)

54. "Collaborative Research: SHF: Small: Efficient and Scalable Privacy- Preserving Neural Network Inference based on Ciphertext-Ciphertext Fully Homomorphic Encryption, **National Science Foundation**, $325k, (April 2023 - March 2026)

55. "Reconfigurable Spectrogram Energy Detector and MIMO Channel Emulator (Recon Spectre-Mice)," **Lockheed Martin Corporation**, $100k, (May 2023 - November 2023)

Technical Society Activities: Organizational

1. Member, Board of Governors, IEEE Circuits and Systems Society (2005, 2006, 2007)
2. Member, IEEE CAS Society (CASS) Fellow Selection Committee (2003, 2004, 2008, 2015, 2017)
3. Member, IEEE CASS Charles A. Desoer Technical Achievement Award Committee (2018)
4. Chair, IEEE CASS Charles A. Desoer Technical Achievement Award Committee (2019)
5. Chair, IEEE CASS John Choma Education Award Committee (2024)
6. Chair, VLSI Systems and Applications Technical Committee, IEEE Circuits and Systems Society (2002-2004)
7. Member, IEEE CASS Outstanding Young Author Award Committee (2003)
8. Member, IEEE Darlington and Guillemin-Cauer Prize Paper Committee (2004, 2005)
9. Member, IEEE CASS Charles A. Desoer Technical Achievement Award Selection Committee (2018, Chair 2019)
10. Chair, ASEE Frederick Emmons Terman Award Selection Committee (2005)
11. Judge, IEEE Fellow Committee, 1998, 1999
12. Judge, ASP-DAC Best Paper Selection Committee (1998)
13. Member, IEEE VLSI Trans. EIC Selection Committee (2002)
14. Editor-in-Chief, IEEE Circuits and Systems Magazine (2024-25)
15. Editor-in-Chief, IEEE Trans. on Circuits and Systems, Part-I: Regular Papers, Jan. 2004-Dec. 2005
16. NSF Panel, 1993, Feb. 2002, Apr. 2003, Dec. 2004, March 2010, Oct. 2011, May 2012, May 2014, June 2014, May 2015, 2017, Aug. 2019, July 2020, March 2021, June 2023
17. (Biomedial Imaging/Engineering) NIH R43/44 Panel, March 2011, March 2012
18. Judge, Davidson Fellowship Selection, 2011, 2012
19. Associate Editor, IEEE Trans. on Circuits and Systems (1990-1991)
20. Associate Editor, IEEE Transactions on Signal Processing (1993-1995)
21. Associate Editor, IEEE Circuits and Systems Trans., Part II: Analog and Digital Signal Processing, 1995-1997
22. Associate Editor, IEEE Trans. on VLSI Systems, 1997-9

23. Associate Editor, IEEE Signal Processing Letters, 1997-1999

24. Editor, Journal of VLSI Signal Processing, 1993-

25. Guest Editor, Special Issue on 1995 IEEE VLSI Signal Processing Wksp. for the Journal of VLSI Signal Processing, Vol. 16(1), May 1997

26. Guest Coeditor, Special Issue on "Theory and Application of Filter Banks and Wavelets", IEEE Trans. on Signal Processing, April 1998

27. Guest Editor, Special Issue on ASAP Conf. 1996 for the Journal of VLSI Signal Processing, Vol. 19(2), June 1998

28. Guest Co-Editor, Special Issue on Interconnect for the Journal of Analog Circuits and Signal Processing, Vol. 31, No. 3, June 2002

29. Guest Co-Editor, Special Issue on SIPS-2002 for the Journal of VLSI Signal Processing

30. Guest Co-Editor, Special Issue on Signal Processing for Broadband Access Systems: Techniques and Implementations for the EURASIP Journal on Applied Signal Processing (Dec. 2003)

31. Associate Editor, IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing, 2002-2003

32. Member, Editorial Board, IEEE Signal Processing Magazine (2003-2006)

33. General Chair, IEEE Signal Processing Systems (SiPS): Design and Implementation Workshop, Oct. 2002

34. International Coordination Chair of IEEE APCCAS 2004, Tainan, Taipei

35. Technical Program Cochair, IEEE VLSI Signal Processing Workshop, Oct. 1995

36. Technical Program Cochair, Applications Specific Array Processors, Sept. 1996

37. Track Chair, Parallel Processing Track, IEEE ISCAS - 1993

38. Track Chair, DSP Processing Track, IEEE ISCAS - 1995

39. Track Chair, VLSI Track, IEEE ISCAS - 2002, 2003

40. Track Chair, VLSI Track, Midwest Symp. on VLSI, 2004

41. Technical Program Committee, IEEE PAINE: International Conference on Physical Assurance and Inspection of Electronics: 2020, 2021, 2022

42. Technical Program Committee, IEEE HOST, 2016, 2017

43. Technical Program Committee (Associate Editor), IEEE EMBC: 2021, 2022

44. Technical Program Committee, ETTIS: Int. Conf. on Emerging Trends and Technologies on Intelligent Systems: 2021, 2022

45. Technical Program Committee: IEEE Conference on Electrical, Electronics, and Computer Engineering (UPCON), 2021

46. Technical Program Committee, Asilomar Conference on Signals, Systems and Computers, 2015

47. Technical Program Committee: IEEE VLSI SP Workshop, 1990 - 96

48. Technical Program Committee: IEEE SiPS Workshop, 1997 - 2004, 2010, 2012, 2020, 2021, 2022

49. Technical Program Committee: IEEE ICASSP 1991 - 2004

50. Technical Program Committee, European Signal Processing Conference (EUSIPCO), 2008

51. Technical Program Committee: IEEE ISCAS 1992 - 93, 1995 - 2002, 2010, 2012 [Track-Chair: 1993 (Parallel Processing), 1995 (DSP), 2002, 2003 (VLSI)]

52. Technical Program Committee, Int. Workshop on System-on-Chip (2003, 2004, 2005)

53. Technical Program Committee, Int. Symp. on System-on-Chip (2003, 2004)

54. Technical Program Committee: IEEE Symp. on Computer Arithmetic, 1997, 2016

55. Technical Program Committee: IEEE ASP-DAC Conference, 1998, 2000

56. Technical Program Committee: ASAP Conf., 1992 - 96, 2002, 2004

57. Technical Program Committee: Great Lakes Symp. on VLSI, 1996, 1999, 2000, 2001, 2003, 2004, 2005, 2006

58. Technical Program Committee: Int. Conf. Electronics, Circuits and Systems (ICECS), Rhodes (Greece), 1996

59. Technical Program Committee: Int. Workshop on Image and Signal Processing, Advances in Computational Intelligence, 1996

60. Technical Program Committee: IEEE Wksp. on VLSI for Communications, 1993

61. Technical Program Committee: Workshop on CORDIC-related Paradigm to Signal Processing Problems, 1998

62. Technical Program Committee: INDICON-2004 (Kharagpur, India)

63. Session Organizer, IEEE DSP Conference, 2015

64. Registration Chair, 1993 IEEE ICASSP Conference (Minneapolis)

65. Advisory Board, 2014 International Conference on VLSI and Signal Processing, Jan. 2014, IIT Kharagpur, India

66. Advisory Board, 1st International Conference on Automation, Control, Energy and Systems, Feb. 2014, Hooghly, India

67. Session Chair, IEEE EMBC Conference, 2012, 2015, 2018

68. Session Chair, Asilomar Conference - 1998, 2001, 2012, 2015, 2017

69. Session Chair, IEEE ICASSP 91, 96, 99, 00, 2015

70. Session Chair, IEEE ISCAS 1992, ISCAS 1993, 1995, 1996, 1997, 1998, 2001, 2002, 2017, 2020

71. Session Chair, IEEE VLSI Signal Processing Workshop, 1992, 1993, 1995, 1996

72. Session Chair, IEEE SiPS Workshop, 1997, 2001

73. Session Chair, IEEE Workshop on VLSI in Communications, 1993

74. Session Chair, 3rd Int. Conf. on Image and Signal Processing, 1995

75. Session Chair, ASAP Conf., Aug. 1994, 1996

76. Session Chair, IEEE ASP-DAC Conf., Jan. 2000

Technical Society Activities: Reviews

1. Ph.D. Thesis Committee, I.I.T. Madras, India, June 2021
2. Ph.D. Thesis Committee, Indian Institute of Science, Bengaluru, India, Aug. 2021
3. Ph.D. Thesis Committee, Indian Institute of Technology, Guwahati, Dec. 2021
4. Ph.D. Thesis Committee, Univ. of Otago, New Zealand, October 2021
5. Ph.D. Thesis Committee, Univ. of Saskatchewan, Saskatoon, Canada, Sept. 2019
6. Ph.D. Thesis Committee, Univ. of Grenoble, France, Feb. 1995
7. Ph.D. Thesis Committee, I.I.T. Bombay, India, Feb. 1998
8. , Ph.D. Thesis Committee, KJIST Univ., Korea (2003)
9. Ph.D. Thesis Committee, Linkoping Univ., Sweden (2003)
10. Ph.D. Thesis Committee, Univ. of Toronto, Canada, 2005
11. Ph.D. Thesis Committee, Univ. of Toronto (2003)
12. Ph.D. Thesis Opponent, Linkoping University, Sweden (2004)
13. Ph.D. Thesis Opponent, Lund University, Sweden (2012)
14. Ph.D. Thesis Examiner, Univ. Canterbury, New Zeland, 2015, 2016, 2018, 2019
15. Ph.D. Thesis Examiner and Committee, Univ. Calgary, Canada, 2015
16. Ph.D. Thesis Examiner and Committee, Indian Institute of Technology, Bhubaneswar, 2017
17. Ph.D. Thesis Examiner, National Institute of Technology, Meghalaya, 2018, 2020
18. Ph.D. Thesis Examiner, National Institute of Technology, Surathkal, 2020
19. Book Reviewer, Kluwer Academic Press, 1990-, McGraw Hill, 1992-, IEEE Press, 1993-, IEEE Comp. Society Press (1994-), CRC Press (2017-), Oxford University Press
20. Reviewer Swiss National Science Foundation (2013)(2015)(2017)(2020)
21. Reviewer, MITACS, Canada, 2020
22. Reviewer, United Arab Emirates University (UAEU), 2020
23. Reviewer, NYU Abu Dhabi Research Proposal, 2018
24. Reviewer, Singapore-MIT Alliance for Research and Technology, 2018
25. Italian Research Assessment Exercise VQR 2004-2010 (2013) (2015)

26. Reviewer, NSF Proposals (1989-), ARO Proposals (1992-), UK EPSRC
27. Reviewer, Nature, 2021
28. Reviewer, Nature Communications, 2020
29. Reviewer, Nature Biomedical Engineering, 2017
30. Reviewer, Nature Pediatrics, 2015
31. Human Brain Mapping, 2018
32. Reviewer, NeuroImage, 2016-
33. Reviewer, NeuroImage Clinical, 2018
34. Reviewer, Journal of Neuroscience Methods, 2020
35. Reviewer, IEEE Trans. NanoBio Science, 2017-
36. Reviewer, Clinical EEG and Neuroscience, Sage, 2014-
37. Reviewer, Int. Journal of Neural Systems (IJNS), 2020
38. Reviewer, EURASIP Journal on Advances in Signal Processing, 2014-
39. Reviewer, Royal Society Interface, 2015
40. Reviewer, European Archives of Psychiatry and Clinical Neuroscience (EAPC), 2017
41. Reviewer, IEEE Proceedings, 1986-
42. Reviewer, IEEE Transactions on Circuits and Systems, 1986-
43. Reviewer, IEEE Transactions on Circuits and Systems, Part II, 1993-
44. Reviewer, IEEE Transactions on Circuits and Systems, Part I, 1996-
45. Reviewer, IEEE Trans. Neural Systems and Rehabilitation Engineering, 2018-
46. Reviewer, IEEE Transactions on Computers, 1987-
47. Reviewer, IEEE Journal of Solid State Circuits, 1990-
48. Reviewer, IEEE Trans. on Acoustics, Speech, and Signal Processing, 1989-
49. Reviewer, IEEE Trans. on Parallel and Distributed Systems, 1991-
50. Reviewer, IEEE Trans. on Circuits and Systems for Video Technology, 1991-
51. Reviewer, IEEE Trans. on VLSI Systems, 1993-
52. Reviewer, IEEE Trans. on Image Processing, 1994-

53. Reviewer, IEEE Trans. on Speech and Audio Processing, 1997-

54. Reviewer, IEEE Trans. on Vehicular Technology, 1996-

55. Reviewer, IEEE Signal Processing Letters, 1995-

56. Reviewer, IEEE Signal Processing Magazine, 1997-

57. Reviewer, IEEE Trans. Signal Processing , 1997-

58. Reviewer, IEEE Trans. on Communications, 1996-

59. Reviewer, IEEE Journal of Selected Areas in Communications, 1999-

60. Reviewer, IEEE Trans. on Computer Aided Design, 1999-

61. Reviewer, IEEE Transactions on Cognitive and Developmental Systems (TCDS), 2019-

62. Reviewer, IEEE Trans. on NanoBioScience, 2017
    Reviewer, IEEE Trans. on Emerging Technologies in Computing, 2016, 2018

63. Reviewer, IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2017-

64. Reviewer, IEEE Sensors Journal, 2018

65. Reviewer, IEEE Embedded Systems Letters, 2016

66. Reviewer, IEEE Open Journal on Circuits and Systems (OJCAS), 2021-

67. Reviewer, IEEE Trans. Neural Networks and Learning Systems (TNNLS), 2021-

68. Reviewer, IEEE Trans. Medical Imaging, 2013-

69. Reviewer, IEEE Trans. Biomedical Engineering, 2014-

70. Reviewer, IEEE Trans. Biomedical Circuits and Systems, 2017, 2020

71. Reviewer, IEEE Signal Processing Magazine, 2020

72. Reviewer, IEEE Design and Test Magazine, 2020

73. Reviewer, Frontiers in Neuroscience, 2021-

74. Reviewer, IEE Electronics Letters, 2017

75. Reviewer, PLOS One, 2015-

76. Reviewer: IEICE

77. Reviewer, Elsevier Signal Processing, 2012, 2020

78. Reviewer, ACM TODAES, 1996-

79. Reviewer, Journal of Parallel and Distributed Computing, 1988-
80. Reviewer, Journal of VLSI Signal Processing (Kluwer Academic), 1988-
81. Reviewer, Journal of System Integration (Kluwer Academic), 1991-
82. Reviewer, Multidimensional Systems and Signal Processing (Kluwer), 1994-
83. Reviewer, The Computer Journal, 1993-
84. Reviewer, Applied Mathematics Letters, 2002-
85. Reviewer, Int. Journal of Circuits, Systems and Computers, 1997
86. Reviewer, IEE Proceedings, Circuits, Devices and Systems, 1994-
87. Reviewer, IEEE International Symposium on Circuits and Systems, 1986-
88. Reviewer, Int. J. of Computers and Mathematics, 2001-
89. Reviewer, IEEE Int. Conf. on Acoustics, Speech, and Signal Processing, 1990-
90. Reviewer, IEEE Int. Symposium on Computer Architecture, 1990-
91. Reviewer, IEEE Workshop on VLSI Signal Processing, 1990-
92. Reviewer, IEEE International Parallel Processing Symposium, 1991-
93. Reviewer, IEEE Asia Pacific Conference on Circuits and Systems, 1992 -
94. Reviewer, ACM/IEEE Design Automation Conference, 1991-
95. Reviewer, IEEE Int. Conf. on Image Processing, 1995-
96. Reviewer, International Conference on Parallel Processing, 1988-
97. Reviewer, Int. Conference on Applications Specific Array Processors, 1990-
98. Reviewer, Hawaii International Conference on System Sciences, 1991
99. Reviewer, European Conf. on Circuit Theory and Design, 1993-
100. Reviewer, Midwest Symp. on Circuits and Systems, 1995-
101. Reviewer, Int. Conf. on VLSI Design, 1994-
102. Reviewer, European Signal Processing Conference (EUSIPCO), 1998, 2020
103. Reviewer, IEEE Globecom Conf., 2001, 2003, 2018
104. Reviewer, Percom 2004
105. Reviewer, VTC-2004

106. Reiewer, IEEE ECCTD 2009
107. Reviewer, IEEEE SiPS Workshop, 2009, 2012, 2017
108. Reviewer, Asilomar Conference on Signals, Systems and Computers, 2020
109. Reviewer, IEEE EMBC Conference, 2018, 2019, 2020, 2021, 2022
110. Reviewer, IEEE BioCAS Conference, 2018, 2022
111. Reviewer, IEEE ICC Conference, 2016, 2017
112. Reviewer, IEEE ICECS Conference, 2016

Technical Society Activities: Membership

1. Fellow of IEEE – Circuits and Systems Society (CASS), Signal Processing Society, Computer Society, Engineering in Medicine and Biology Society and Communications Society

2. Member, Technical Committee on VLSI Systems and Applications, IEEE CAS Society (Chair-Elect: 2000-2002, Chair: 2002-2004)

3. Member, Tech. Cmt. on Visual Signal Processing and Communications, IEEE CAS Society (retired)

4. Member, Tech. Cmt. on Digital Signal Processing, IEEE CAS Society (retired)

5. Founding Member, Tech. Cmt. on Nanoelectronics and Gigascale Integration, IEEE CAS society (retired)

6. Member, Technical Committee on Design and Implementation of SP Systems, IEEE Signal Processing Society (1990-1996, Advisory Member, 1996-)

7. Member, Technical Committee on VLSI, IEEE Computer Society

University Activities

1. Director of Graduate Stuides (2008-2011)

2. MN Future Proposal Review Panel (2013)

3. Graduate Teaching Award Selection Committee (2014, 2015, 2016)

4. Dosdall Fellowship Evaluation Committee (2012)

5. McKnight - Land Grant Professor Selection Committee (2018-2021)

6. Interdisciplinary Doctoral Fellowship Selection Committee (2019-2023)

7. Shevlin Fellowship Selection Committee (2018-2019)

8. Member, Graduate Education Committee, Graduate School (2012)

9. CSE Awards Committee (2022-2023)

10. Chair, Graduate Standards Committee (2007-2008)

11. Member, Graduate Standards and Program Committee, Electrical Eng. Dept. (1989-90) (1997-98) (2003-2004)

12. Member, Faculty Recruiting Committee of Electrical & Computer Eng. Dept. (1990-95) (1998-99)(2002-03)(2004-2005)(2005-2006) (2011-2012) (2012-2013)(2016-17) (2019) (Chair 2021-22) (2022-2023)

13. Member, Faculty Promotion and Tenure Committee of Electrical Eng. Dept. (1995-96) (1998-99) (2013-14) (Chair, 2017-2018) (2019-20) (Chair, 2020-2021)

14. Member, Ph.D. Written Qual. Exam. Committee (1989, 1990, 1998, 2002-3, 2004-5, 2009-10, 2012-13) (2015) (2017-2018)

15. Member, ECE 7.12 Committee, 2022-2023

16. Member, Space Committee (2014-2016)

17. Instructor for Oral Presentation Training (1990)

18. Member, *Adhoc* Committee on Ph.D. Written Examination, 1993

19. Chair-Systems and Hardware Track for Univ. Digital Summit (1997)

Post Doctoral Fellows and Visitors Supervised

1. Kazuhito Ito, Currently Professor, University of Saitama, Japan (1992-1993)
2. Ching-Yi Wang, Currently with Boston Scientific (1993-1996)
3. Luis Montalvo, Currently with Technicolor, France (1995-1996)
4. Michael Zervakis, Currently Professor at Technical Univ. of Crete, Chania, Crete, Greece (1996)
5. Steve Summerfield, Formerly with Univ. of Warwick, Coventry, U.K., Currently with Huawei, London (1997)
6. Hiroshi Suzuki, Curretly Senior Manager at Broadcom Limited, Irvine, CA (1997-1999)
7. Javier Valls, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
8. Trini Sansaloni, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
9. Yuke Wang, Currently Patent Lawyer (Dallas, Texas) (1999)
10. Jin-Gyun Chung, Currently Dean of Engineering, Chonbuk National Univ., Korea (2001)
11. Chester Park, Currently Asst. Prof. at Konkuk University, Korea (2005)
12. Chunlei Xia (Shanghai, China, 2006)
13. Mario Garrido, Currently Asst. Professor at Universidad Politecnica de Madrid (UPM) (20070
14. Hemant Patil, Currently Assoc. prof. at DA-IICT, Gandhinagar, India (2009)
15. Xiaoping Li, Nanjing Univ, China (2010)
16. Sayed Ahmad Salehi, Currently Asst Prof. at Univ. of Kentucky (2011-12)
17. Yun-Nan Chang, Currently Professor at National Sun Yat-Sen Univ., Taiwan (2012)
18. Mojtaba Bandarabadi, Currently with Inselspital Bern, Switzerland (2012) (coadvised by Dr. Tay Netoff)
19. Abdolreza Rashno, Predoctoral Visitor from Isfahan University of Technology, Iran, 2016-2017
20. Sai Sanjeet, Predoctoral Visitor from Indian Institute of Technology, Kharagpur, India, 2023
21. Weihang Tan, Postdoctoral Research Associate, 2023, Currently with ScaleFlux

Ph.D. Theses Supervised

1. Lori E. Lucke, "Applying Parallel Processing Techniques to Digital Signal Processing Algorithms and Architectures for High Level VLSI Synthesis", December 1992

   [Currently Fellow, Minnetronix Corp, St. Paul]

2. Ching-Yi Wang, "MARS: A High-Level Synthesis Tool for Digital Signal Processing Architecture Design", December 1992

   [Currently with Boston Scientific, St. Paul]

3. Naresh R. Shanbhag, "Design of Pipelined VLSI Adaptive Digital Filters with Relaxed Look-Ahead", July 1993

   [Currently Jack kilby Professor at Univ. of Illinois at Urbana]

4. H.R. Srinivas, "Floating Point Computer Arithmetic Architectures", September 1994

   [Currently Senior Manager, Broadcom limited, Irvine, CA]

5. K.J. Raghunath, "Pipelined STAR RLS Adaptive Filters", October 1994

   [Currently Principal Architect, Ikanos Communications, NJ]

6. Jin-Gyun Chung, "Pipelined IIR Lattice and Wave Digital Filters", November 1994

   [Currently Professor at Chonbuk National University, Chonju, South Korea]

7. Tracy C. Denk, "Retiming, Folding and Register Minimization", July 1996

   [Currently CEO and Cofounder, First Fidelity Funding Group (FFFG), Irvine, CA]

8. Janardhan H. Satyanarayama, "Design of Low-Power DSP Systems", March 1998

   [Currently with Intel, PA]

9. Ahmed Shalash, "Architecture and System Design for Digital Subscriber Loop Communications", June 1998

   [Currently Professor at Cairo University, Egypt, Retired]

10. Leilei Song, "Low-Power VLSI Architectures for Finite-Field Applications", June 1999

    [Currently at Apple, Cupertino, CA]

11. Yun-Nan Chang, "Low-Power Bit-Serial and Digit-Serial DSP Systems", June 1999

    [Currently Professor at National Sun Yat-Sen University, Kaohsiung, Taiwan]

12. Jun Ma, "Pipelined RLS Adaptive Filters", July 1999

13. Martin Kuhlmann, "High-Performance Low-Power Arithmetic, Architectures and Circuits", Dec. 1999

    [Passed Away March 2018; Formerly Director at Inphi, Irvine, CA]

14. Vijay Sundararajan, "Performance Optimization Methodologies for Design of Digital VLSI Systems", Jan. 2000

    [Currently Director at Broadcom Inc., San Jose, CA]

15. Zhongfeng Wang, "High-Performance and Low-Cost VLSI Design of Turbo Decoders", Aug. 2000

    [Currently Full Professor at Nanjing University, China]

16. Robert A. Freking, "Structural Strategies for High-Performance Undelimited-Codeword Source Coding", October 2000

    [Currently with MIT Lincoln Laboratories]

17. William L. Freking, "Algorithms and Architectures for High-Performance Public-Key Cryptography Systems", October 2000

    [Currently with MIT Lincoln Laboratories]

18. Lijun Gao, "Architecture Design and Mapping of DSP Systems", Feb. 2001

    [Currently with Analog Devices, Boston]

19. Zhipei Chi, "High Performance, High Speed VLSI Architectures for Wireless Communication Applications", June 2001

    [Currently with NXP]

20. Tong Zhang, "Efficient VLSI Architectures for Error Correction Coding", June 2002

    [Currently Full Professor of ECSE Dept., R.P.I., Troy, NY]

21. Yanni Chen, "Low-Complexity High-Speed VLSI Architectures for Error-Correction Decoders", June 2003

    [Currently at Apple, Cupertino, CA]

22. Junjin Kong, "Classical and Quantum Convolutional Codes: Design and Implementation", Feb. 2005

    [Currently a "Master" at Samsung, S. Korea]

23. Xinmiao Zhang, "Architectures for Error Control Coders and Cryptography Systems", June 2005

    [Tenured Prof. at The Ohio State Univ.]

24. Yongru Gu, "VLSI Architectures for High-Speed Transceivers", July 2005

    [Cofounder of Startup Inplay Tech, Irvine]

25. Jun Tang, "Architectures for OFDM Based Ultra Wideband Systems", July 2006

    [Cofounder of Startup Inplay Tech, Irvine, CA]

26. Sangmin Kim ,"Efficient VLSI Architectures for Error Control Coders", Oct. 2006

    [Currently with Qualcomm, San Diego]

27. Jianhung Lin, "Algorithm and Architectures for Next Generation Multimedia Systems", Jan. 2007

    [Currently with Marvell, CA]

28. Yuping Zhang, "VLSI Architectures for Turbo Code Decoder, LDPC Code Decoder and List Sphere Decoder", May 2007

    [Currently with Marvell, CA]

29. Chao Cheng, "High-Speed Low-Cost VLSI DSP Algorithms Based on Novel Fast Convolutions and Look-Ahead Pipelining Structures", May 2007

    [Currently with Tiktok, CA]

30. Aaron E. Cohen, "Architectures for Cryptography Accelerators" September 2007

    [Currently with Naval Research Lab, Washington, DC]

31. Daesun Oh, "Low Complexity VLSI Architectures for LDPC Decoders", May 2008

    [Currently with Samsung, S. Korea]

32. Jie Chen, "Efficient VLSI Architectures for High-Speed Ethernet Transceivers", Aug. 2008

    [Currently Cofounder and VP of Data Storage Technology at InnoGrit Corporation. Santa Clara, CA]

33. Renfei Liu, "Error Control Algorithms and Architectures for Reliable DSP Systems", Nov. 2010

    [Currently with Broadcom Corp., Irvine, CA]

34. Yun Sang Park, "Reduced-Complexity Epileptic Seizure Prediction with EEG," Jan. 2012 (Coadvised by Prof. Theoden I. Netoff)

    [Currently with Samsung, S. Korea]

35. Hua Jiang, "Digital Logic and Signal Processing Computations with Molecular Reactions," May 2012 (Coadvised by Prof. Marc D. Riedel)

    [Currently with Netflix, CA]

36. Manohar Ayinala, "Low-Power Architectures for Signal Processing and Classification Systems," July 2012

    [Currently with Intel, Austin, TX]

37. Chuan Zhang, "Low-Latency Low-Complexity Channel Decoder Architectures for Modern Communication Systems," December 2012

    [Currently Professor at Southeast University, China]

38. Te-Lung Kung, "Synchronization and Coding in Wireless Communication Systems," September 2013

39. Sohini Roychowdhury, "Automated Segmentation and Pathology Detection in Ophthalmic Images," July 2014

    [Currently with Fourth Brain, CA]

40. Yingjie Lao, "Authentication and Obfuscation of Digital Signal Processing Integrated Circuits," July 2015

    [Currently Assistant Professor at Clemson University, South Carolina]

41. Bo Yuan, "Algorithm and Architecture for Polar Codes Decoder," July 2015

    [Currently Assistant Professor at Rutgers University, NJ]

42. Tingting Xu, "Biomarkers for Mental Disorders from Neuroimaging Data," December 2016

    [Currently with Ad Colony, Seattle]

43. Yin Liu, "Digital Signal Processing and Machine Learning System Design using Stochastic Logic," July 2017

    [Currently with Snapchat, Redmond, WA]

44. Sayed Ahmad Salehi, "A Framework for Computing Discrete-Time Systems and Functions using DNA," July 2017 (Coadvised by Prof. Marc D. Riedel)

    [Currently Assistant Professor at University of Kentucky]

45. Zisheng Zhang, "Approaches to Feature Identification and Feature Selection for Binary and Multi-Class Classification," July 2017

    [Currently with iRhythm, San Francisco]

46. Sandhya Koteshwara, "Secure, Resilient and Low-Energy Hardware Architectures for Internet-of-Things," September 2018

    [Currently with IBM T.J. Watson Research Center, Yorktown Heights, NY]

47. Shu-Hsien Chu, "pproaches to Anatomical and Functional Brain Connectivity Analysis with Applications to Adolescent Major Depressive Disorder," September 2018 (Coadvised by Prof. Christophe Lenglet)

    [Currently with Intel, Oregon]

48. Bhaskar Sen, "Static and Dynamic Connectivity Analysis of Human Brain via Functional Magnetic Resonance Imaging," July 2020

    [Currently with Microsoft, Redmond, WA]

49. Satya Venkata Sandeep Avvaru, "Novel Methods for Causal Network Analysis in the Human Brain: Applications in Cognitive Control and Parkinson's Disease," April 2022

    [Currently with Neuromodulation Group, Boston Scientific, Houston]

50. Nanda Kumar Unnikrishnan, "Towards Hardware-Software Co-design for Energy-Efficient Deep Learning," June 2023

    [Currently with Meta, Menlo Park, CA]

51. Xingyi Liu, "Machine Learning Systems Design using Molecular and DNA Reactions," August 2023

    [Currently with Mayo Clinic, Rochester, MN]

52. Lulu Ge, "Hyperdimensional Computing based Classification and Clustering: Applications to Neuropsychiatric Disorders," December 2023

M.S. Projects Supervised

1. Gregory S. Munson, "Finite Precision Effects in Scattered and Clustered Look-Ahead Pipelined Recursive Digital Filter Implementations", June 1989

   [Currently with JAMF Software, Eau Claire, WI]

2. Jim Malaney, "Design of a Programmable Digital Filter", November 1989

   [Manager at GE Healthcare, Madison, Wisconsin]

3. Lai Q. Pham, "Roundoff Error in Digital Filters using Redundant Numbers", November 1989

4. Syed Babar Raza, "Reduction of Hardware Overhead in Recursive Filters by Interleaving", January 1991

5. Joo-Sang Lee, "A New Approach For Design Of Data Format Converter Architectures Using Register Allocation", May 1991

   [Currently with Micron Technology, Dallas, TX]

6. H.R. Srinivas, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", July 1991

   [Currently Senior Manager at Broadcom, Irvine, CA]

7. N. Iyer, "iSchematic: An Automatic Schematic Generator for OCT 5.0 Data Base", September 1991

8. Andrew P. Brown, "Applications of Circuit Retiming to DSP Architecture Design", October 1991

   [Currently with MBA Engineering, MN]

9. J.-G. Chung, "Synthesis of Pipelined Lattice IIR Digital Filter", November 1991

   [Currently Dean of Engineering, Chonbuk National Univ., S. Korea]

10. Gireesh Shrimali, "Fast Arithmetic Coder Architectures", June 1993

11. Wayne C. Amendola, Jr., "VLSI Implementation of a 200 MHz 16X16 Redundant Digit Multiplier and a 125 MHz 16X16 Booth-Encoded Redundant Digit Multiplier", June 1993

    [Currently Data Analyst, Capital One, CA]

12. Bin Fu, "VLSI Design Advances in Arithmetic Coding", May 1995

13. Santosh Misra, "CDMA Based Mobile Communication Systems", May 1995

    [Indian Administrative Service (IAS), Officer, Govt. of Chhattisgarh, India]

14. Darren Pearson, "Low Power Strategies for VLSI Implementation of Digital Filters", May 1995

    [Currently Instructor at St. Paul College, MN]

15. Surendra Jain, "Efficient VLSI Architectures for Finite Field Arithmetic", June 1995

    [Currently Venture Capitalist, Bengaluru, India]

16. Yun-Nan Chang, "High-Level DSP Synthesis using Heterogeneous Functional Units", June 1995

    [Currently Professor at National Sun Yat-Sen University, Taiwan]

17. Yuet Li, "STAR Adaptive Lattice Recursive Least Square Filters", February 1996

    [Currently Associate Technical Director at Broadcom, Fremont, CA]

18. Chong Xu, "Power-Speed Reconfigurable FIR Filters", February 1996

    [Currently with Intel, CA]

19. David A. Parker, "Low-Area/Power Parallel FIR Filters", May 1996

    [Currently Director at Altera, CA]

20. Mayukh Majumdar, "Low-Area Data Format Converters", June 1996

21. Leilei Song, "Efficient Bit-Serial Finite Field Multipliers", June 1996

    [Currently at Apple, Cupertino, CA]

22. John Bratt, "VHDL Interface for MARS DSP Synthesis System", June 1996

    [Currently with AMD, CO]

23. Hojun Kim, "Coefficient Optimization in Pipelined IIR Digital Filters", July 1996

    [Currently with Telematics, CA]

24. Mousumi Gayen, "ILP Scheduling with Processor Interconnection", Jan. 1997

25. Nikhil Sarpotdar, "Radix-2 Division and Square Root Algorithms: Study and Implementation", July 1997

26. William Ho, "Power Efficiency of the Carry-Select Adder", August 1997

    [Currently with a Startup, CA]

27. Ashish Karandikar, "Low-Power and High-Performance Static Random Access Memory", December 1997

    [Currently Vice President, Nvidia]

28. Zhipei Chi, "Pipelined Single and Multi-Channel Lattice RLS Adaptive Filters", Sept. 1998

    [Currently with Marvell, CA]

29. Nidish Kamath, "Scheduling of DSP Algorithms for Low-Power Design", Jan. 1999

    [Currently Technologist, Bay Area, CA]

30. Dhiraj Kumar, "Performance Tradeoffs of DCT Architectures in Xilinx FPGAs", April 1999

    [Currently Senior Director at Paypal, NY; Previously Sales Executive, Facebook]

31. Ziyu Li, "DLMS Adaptive FIR Filter: Bit-Serial Systolic Array VLSI Implementation", July 1999

    [Predictive Modeling Analyst at Travelers, MN]

32. Robin Bansal, "Optimized Power and Delay Solutions for Digital CMOS Circuits by Transistor Reordering using HEAT", August 1999

    [President and CEO, Bansi Holdings, PA]

33. Ru-Guang Chen, "Double Error Correction on Residue Number System", Feb. 2000

    [Currently with Amazon, CA]

34. Bibhudatta Sahoo, "A Low Power Correlator", Aug. 2000

    [Currently Associate Professor in Amrita University, Bengaluru, India]

35. Siwei Chen, "Minimal Switching Activity Schedules for Various FIR Filters", Aug. 2000

    [Currently with Focaltech, Providence, RI]

36. Wenhao Wu, "VLSI Design and Implementation of Two Viterbi Decoders", Aug. 2000

    [Currently with Intel, CA]

37. Karuna Prasad, "Power Analysis of 4-2 and 5-2 Compressors", Jan. 2001

38. Aaron E. Cohen, "VLSI Architectures for RSA," June 2004

    [Currently with Naval Research Lab, Washington, DC]

39. Saurabh Jain, "Low-Complexity Pipelined-Parallel Decision Feedback Decoder (PDFD) for 1 Gbps Ethernet", August 2004

    [Currently with Marvell, CA]

40. Lina Long, "A VLSI Implementation for Viterbi Decoder in Ultra Wide-band System", March 2005

    [Currently with Cisco, CA]

41. Manoj Yadav, "LDPC Decoder for DVB System", May 2005

    [Currently Manager at Marvell, CA]

42. Renfei Liu, "VLSI Architectures for Viterbi Decoders," May 2007

    [Currently at Broadcom, Irvine, CA]

43. Daesun Oh, "LDPC Decoder Architectures," Feb. 2008

    [Currently with Samsung, S. Korea]

44. Jie Chen, "Architectures for 10-Gigabit Ethernet," Feb. 2008

    [Currently Cofounder and VP of Data Storage Technology at InnoGrit Corporation. Santa Clara, CA]

45. Priyadharshini Vijayakumar, "Timing Variations in Digital Filters with Supply Voltage Variations", Aug. 2008

    [Currently with Intel, CA]

46. Prashant Metkar, "Improved Approach for Calculating Model Parameters in Speaker Recognition using Gaussian Mixture Models", May 2009

    [Currently Financial Engineer in Pune, India]

47. Jaime Rivera, "Research for the Development of an Apparatus To Help Prevent Sudden Infant Death", May 2009

    [Currently with Eagle Properties, Rochester, MN]

48. Xiaoming Zhu, "Lung Sound Separation by Independent Component Analysis", June 2009

    [Currently at Marvell, CA]

49. Yun-Sang Park, "Seizure Prediction by Support Vector Machine Classification," Jan. 2010

    [Currently with Brown Univ as Postdoc]

50. Yingbo Hu, "Subthreshold Circuit Design", August 2010

    [Currently with Maxim, CA]

51. Manohar Ayinala, "High-Throughput VLSI Architectures for CRC/BCH Encoders and FFT Computations", Nov. 2010

    [Currently with Intel, Allentown, PA]

52. Lan Luo, "Postprocessing of Seizure Prediction by Kalman Filter", May 2011

    [Currently with Google, Mountain View, CA]

53. Te-Lung Kung, "Frame Start Synchronization in OFDM System," September 2011

54. Michael Brown, "A Low-Complexity Seizure Prediction Algorithm," November 2011

    [Currently with Digi Wireless Devices, MN]

55. Chuan Zhang, "Polar Code Decoder Architectures," April 2012
    [Currently Professor at Southeast University, China]
56. Tingting Xu, "Schizophrenia Classification from MEG," May 2013
    [Currently with a University in Nanjing, China]
57. Manikandan Palani, "EEG Data Compression," May 2014
    [Currently with Qualcomm, Denver, CO]
58. Aravinth Chinnapalanichamy, "Serial and Interleaved FFT Architectures for Real Signals," Jan. 2015
    [Currently with Nvidia]
59. Sandhya Koteswara, "Obfuscated FFT Architecture," Feb 2015
    [Currently IBM T.J. Watson Research Center, Yorktown Heights]
60. Sayed Ahmad Salehi, "DNA Computing," April 2015
    [Currently with University of Kentucky]
61. Yingjie Lao, "Removing Redundancies of Fast Fourier Transform Computations," July 2015
    [Currently with Clemson Univ., South Carolina)
62. Goutham N. C. Shanmugam, "Obfuscated Real FFT Architecture," August 2015
    [Currently with ARM, Austin, TX]
63. Vaishnavi Santhapuram, "Timing Induced Error Analysis for Wallace Tree Multipliers," Oct. 2015
    [Currently with Intel, CA]
64. Anoop Koyily, "A Study on Modeling of MUX-based Physical Unclonable Functions," April 2018
    [Currently with Apple, San Diego]
65. S.V. Sandeep Avvaru, "Attack-Resistance and Reliability Analysis of Feed-Forward and Feed-Forward XOR Arbiter PUFs," May 2019
    [Currently with Boston Scientific]

Graduate and Undergraduate Advisees

I am currently advising following Visitors, and Students.

1. Sai Sanjay Balaji (Ph.D.)
2. Sin-Wei Chiu (Ph.D.)
3. Wenrui Xu (Ph.D.)
4. Aditya Sodhani (Ph.D.)
5. Ryan Nelson (Ph.D.)
6. Joe Gould (MSECE)
7. Carl Anderson (MSECE)
8. Megan Adamek (NSF REU)
9. Evan Krainess (NSF REU)
10. Ryan Ng (NSF REU)

New Course Development

1. I developed two new classes "VLSI Digital Signal Processing (EE 5329)" and "Digital Signal Processing Structures for VLSI" (EE-5549) in Spring 1989/Spring 1990.
2. I developed and taught the "VLSI Low-Power and Digital Video Systems (EE 8451)" Course in Fall 1997.
3. I developed and taught the "Digital Arithmetic, Error Control Coding and Cryptography Architectures" (EE 5953)" Course in Winter 1999
4. Developed and taught a new class "VLSI Communications Systems" in Spring-2003 (EE-8950)
5. Introduced and Taught "Teaching Experience in EE" class (EE-8920) (2010-11) (Spring 2012) (Spring 2014)
6. Introduced and Taught "Ethics and Professional Conduct in EE" (EE-8925) (Fall-2010) (Spring 2011) (Spring 2013) (Spring 2015) (Fall 2019)
7. I taught a new graduate course on Digital Signal Processing Applications (Spring 2015). Applications from neuroengineering and biomedical signal analysis were emphasized.
8. I taught a new Graduate Course on "Neuromorphic Computing Architectures" (EE-8950) in Fall-2019.
9. I taught a new Graduate Course on "Codesign in Modern Computing" (EE-8950) in Spring-2024.

Tutorials, Short Courses, Panels, Invited Keynote Talks

1. Co-Presenter, Tutorial Workshop on "VLSI DSP Synthesis" at IEEE ICASSP 92 (also available as an *IEEE Video Tutorial*)
2. Presenter, Tutorial on DSP Architectures and Synthesis at VLSI'95
3. Organizer and Copresenter, Tutorial on DSP Architectures and Synthesis at IEEE ISCAS 95
4. Organizer and Copresenter, Tutorial on Design of High-Performance DSP Systems at IEEE ISCAS 96
5. Organizer and Copresenter, Tutorial on High-Performance Video DSP Systems at IEEE ISCAS 97
6. Organizer and Copresenter, Tutorial on Low-Power Multimedia DSP Systems at IEEE ICASSP98
7. Presenter, Tutorial on VLSI Architectures for Video and Data Communications at IEEE ISCAS98
8. Copresenter, Tutorial on Design Methodologies for Low Power Signal Processing, IEEE Int. Symp. on Low Power Electronics and Design, Monterey, Aug. 1998
9. Organizer and presenter, Tutorial on Design of Low-Power Multimedia DSP Systems at IEEE ISCAS 1999
10. Panelist, Future of Digital Signal Processing, ISCAS'96
11. Plenary Talk Speaker, ICVC-97
12. Invited Speaker, IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
13. Panelist, "Single Chip or Multiple Chips", IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
14. Keynote Talk Speaker, 2001 IEEE SiPS Workshop (Antwerp, Belgium)
15. Invited Speaker, 2001 System-on-Chip Conference (Tampere, Finland)
16. Panlist, 2001 System-on-Chip Conference (Tampere, Finland)
17. Invited Speaker, 2003 IEEE SiPS Workshop, Seoul, Korea (August 2003)
18. Tutorial Copresenter, IEEE Portable 2007 Conf.

19. Tutorial Copresenter, IEEE ISCAS 2007 Conf.

20. Keynote Talk "VLSI Systems for Neurocomputing and Health Informatics," Proc. of 2014 ACM Great Lakes Symposium on VLSI, Houston, May 2014

21. Short Course on VLSI Signal Processing, Indian Institute of Technology, Kharagpur, Dec. 2016

22. Short Course on VLSI Communications Systems and Ethernet Transceivers, Indian Institute of Technology, Kharagpur

23. Tutorial Presentation on Hardware Security, IEEE ISCAS, 2017

24. Keynote Speaker, Workshop on Processing for Communication and Intelligent Information (PCII), Fudan University, Shanghai, June 2017

25. Short Course on VLSI Signal Processing, Fudan University, China, June 2017

26. Short Course on Hardware Security: Authentication and Obfuscation, Guru Jambheshwar University of Science and Technology, Hisar, August 2017

27. Tutorial on Data-Driven Healthcare: Applications from Neurology, Psychiatry and Ophthalmology, IEEE ISCAS, 2018

28. Tutorial on Energy-Efficient AI: System Architectures and Computational Models Based on CMOS and Beyond-CMOS Devices (with B. Yuan, N.R. Shanbhag, A. Sebastian and B. Rajendran), 2019 IEEE ISCAS, Sapporo, Japan, May 2019

29. Keynote Talk: "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," IEEE Signal Processing Systems Workshop, Nanjing, China, October 21, 2019

30. Tutorial on Brain Inspired Computing: Models and Architectures, 2020 IEEE ISCAS, Seville, Oct. 2020 (Virtual)

31. One-Day SGort Course for IEEE CASS Africa School Webinar on Brain Inspired Computing, Oct. 2020

32. Keynote Speaker, Asilomar Conference on Signals, Systems and Computers, Nov. 3, 2020

33. "Machine Learning Everywhere: Applications and Low-Energy Architectures," Keynote Talk at ETTIS-2021: Emerging Trends and Technologies on Intelligent Systems, CDAC, Noida, New Delhi, March 4, 2021

34. "Low-Energy Machine Learning Systems: Architectures and Applications" Plenary Talk at the Third Argentinian Conference on Electronics, March 10, 2021

35. "Accelerator Architectures for Deep Neural Networks: Inference and Training," 2021 VLSI Design & Test Conference (VDAT), India Sept. 18, 2021 [Plenary Talk]

36. Short Course on VLSI Signal Processing Systems, Indian Institute of Technology, Bhubaneswar, Feb. 2021

37. Short Course on VLSI Signal Processing Systems, Indian Institute of Technology, Kharagpur, India, July-August 2021

38. Keynote Talk "Hardware Security: Functional Encryption and Homomorphic Encryption Acceleration," Keynote Talk at ETTIS-2022: Emerging Trends and Technologies on Intelligent Systems, CDAC, Noida, New Delhi, March 22, 2022

39. Tutorial on Brain Inspired Computing: Models and Architectures at 2023 IEEE International Conference on Acoustics, Speech, and Signal Processing, Rhodes, Greece, June 2023

40. Tutorial on Quantum Error Correcting Codes and Circuits: Algorithm-Architecture Codesign, 2024 IEEE International Conference on Acoustics, Speech, and Signal Processing, Seoul, S. Korea, April 2024

Non-Conference Invited Talks

1. "Pipelining and Parallel Processing of Recursive Digital Filters," University of California, Santa Barbara, May 1986

2. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Minnesota, Minneapolis, 1988

3. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," IBM T.J. Watson Research Center, Yorktown heights, NY, 1988

4. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," AT&T Bell Laboratories, Holmdel, NJ, 1988

5. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Texas Instruments, Dallas, 1988

6. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Motorola, Austin, Texas, 1988

7. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Bell Communications Research, NJ, 1988

8. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Southern California, Los Angeles, 1988

9. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Michigan, Ann Arbor, 1988

10. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Carnegie Mellon University, Pittsburgh, 1988

11. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Maryland, College Park, 1988

12. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Washington, Seattle, 1988

13. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Wisconsin, Madison, 1988

14. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Yale University, 1988

15. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Pennsylvania, Philadelphia, 1988

16. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," North Carolina State University, Raleigh, 1988

17. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Purdue University, West Lafayette, 1988

18. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Texas-Austin, Austin, 1988

19. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Cornell University, Ithaca, NY, 1988

20. "Multiprocessor Scheduling in Signal Processing Programs," U.S. West Advanced Technologies, Englewood, Colorado, August 1989

21. "Application of Unfolding in Signal Processing Applications," University of Colorado, Boulder, August 1989

22. "CAD of Real-Time DSP ICs," Texas Instruments, Dallas, Feb. 1990

23. "Approaches to High-Speed Digital Signal Processing," National University of Singapore, May 1991

24. "Critical Path Reduction by Unfolding and Folding Techniques," NEC Computer & Communication Lab., Japan, April 1992

25. "High-Speed Digital Signal Processors", NEC Computer & Communication Lab., Japan, May 1992

26. "Dedicated VLSI Digital and Signal Processors", Toshiba (Japan), May 1992

27. "Dedicated VLSI Digital and Signal Processors", Tokyo Inst. of Technology (Japan), May 1992

28. "Dedicated VLSI Digital and Signal Processors", NTT Transmission Laboratory (Japan), May 1992

29. "Dedicated VLSI Digital and Signal Processors", Tohuku University, Sendai (Japan), May 1992

30. "VLSI Wavelet Architectures", NEC Computer & Communication Lab., Japan, June 1992

31. "Dedicated VLSI Digital and Signal Processors", Indian Institute of Technology, New Delhi (India), July 1992

32. "Dedicated VLSI Digital and Signal Processors", Swiss Federal Institute of Technology, Zurich (Switzerland), August 1992

33. "Register Minimization in DSP Architectures", NCUBE Corporation, Bangalore, India, December 1993

34. "High-Speed Multiplication and Addition", IEEE Section, Bangalore, India, December 1993

35. "Pipelined VLSI IIR and Adaptive Digital Filters", Indian Institute of Science, Bangalore, India, December 1993

36. "High-Level Transformations for DSP Synthesis", Indian Institute of Science, Bangalore, India, December 1993

37. "Pipelined VLSI IIR and Adaptive Digital Filters", Department of Electrical Engineering Seminar, University of California, Davis, August 1994

38. "VLSI Architectures for Approximation Algorithms", Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, August 1994

39. "Dedicated VLSI Digital Signal Processors", Department of Electrical and Computer Engineering, University of Iowa, Iowa City, August 1994

40. Lectures on "VLSI Digital Signal Processing," Central Electronics Engineering Research Institute (CEERI), Pilani, India, Dec. 1994

41. Four Lectures on "VLSI Digital Signal Processing," Center for Development of Advanced Computing, Pune, Feb. 1995

42. "Low-Energy Embedded DSP Systems," AT&T Bell Laboratories, July 1995

43. "High-Performance VLSI Digital Signal Processing," Indian Telephone Industries, Bangalore, March 1996

44. Two Lectures on "VLSI Digital Signal Processing," Indian Institute of Technology, New Delhi, March 1996

45. "VLSI Digital Signal Processors", Univ. of Nottingham, U.K. (June 1995)

46. Lectures on "VLSI Digital Signal Processing", Delft Univ. of Technology, March and April 1996

47. "High-Performance VLSI Digital Signal Processing," National Tsing-Hua University, Hsinchu, Taiwan, October 17, 1996

48. "High-Performance VLSI Digital Signal Processing," National Chao-Tung University, Hsinchu, Taiwan, October 18, 1996

49. "High-Performance VLSI Digital Signal Processing," National Taiwan University, Taipei, Taiwan, October 21, 1996

50. "Design and Implementation of Dedicated and Programmable DSP Systems," Univ. of Ryukyus, Okinawa, Jan. 20, 1997

51. "Design and Implementation of Dedicated and Programmable DSP Systems," Kyushu University, Fukuoka, Jan. 21, 1997

52. "Design and Implementation of Dedicated and Programmable DSP Systems," LSI Division, Kawasaki Steel, Makuhari, Feb. 12, 1997

53. "Design and Implementation of Dedicated and Programmable DSP Systems," Technical Group Meeting of IEICE DSP, CAS and CS Groups, March 6, 1997, Hiroshima University

54. "Dedicated and Programmable VLSI Signal Processing Systems," Osaka University, Osaka, Japan, March 31, 1997

55. "Dedicated and Programmable VLSI Signal Processing Systems," Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, April 7, 1997 (IEEE CAS Distinguished Lecture)

56. "Dedicated and Programmable VLSI Signal Processing Systems," K-JIST, Kwanju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)

57. "Dedicated and Programmable VLSI Signal Processing Systems," Chonbuk National University, Chonju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)

58. "Dedicated and Programmable VLSI Signal Processing Systems," Seoul National University, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)

59. "Dedicated and Programmable VLSI Signal Processing Systems," Daewoo Center, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)

60. "Dedicated and Programmable VLSI Signal Processing Systems," Tohoku University, Sendai, Japan, April 18, 1997

61. "Dedicated and Programmable VLSI Signal Processing Systems," University of Southern California, Los Angeles, April 21, 1997 (Invited Talk)

62. "Dedicated and Programmable VLSI Signal Processing Systems," Inst. of Electronics, Academia Sinica, Beijing, China, June 2, 1997 (IEEE CAS Distinguished Lecture)

63. "Dedicated and Programmable VLSI Signal Processing Systems," Tsinghua University, Beijing, China, June 3, 1997 (IEEE CAS Distinguished Lecture)

64. "Dedicated and Programmable VLSI Signal Processing Systems," Tokyo Institute of Technology, Tokyo, Japan, June 30, 1997

65. "VLSI Architectures for High-Performance DSP Systems," University of California at Berkeley, Sept. 19, 1997

66. "Low-Power Digital Signal Processing for Multimedia Systems," University of Minnesota (Colloquim Talk), Oct. 9, 1997

67. "Low-Power VLSI Digital Signal Processing for Multimedia Systems," PLENARY TALK, IEEE Biannual Int. Conf. on VLSI Design and CAD, (ICVC), Oct. 12-15, 1997, Seoul, Korea

68. "Low-Power Arithmetic Components," Intel Corporation, Aug. 13, 1998

69. "Low-Power VLSI Digital Signal Processing Systems," Broadcom Corporation, Irvine, California, Aug. 14, 1998

70. "Low-Power Multimedia DSP Systems," ECE Colloq. talk at University of Illinois at Urbana, Sept. 15, 1998

71. "Low-Power Multimedia DSP Systems," Lucent Technologies, Bell Laboratories, Allentown, PA, Sept. 23, 1998

72. "Low-Power DSP Systems for Multimedia Communications," Texas Instruments, Dallas, Oct. 1, 1998

73. "Low-Power Multimedia DSP Systems," EECS Department, Univ. of California, Berkeley, Nov. 2, 1998

74. "Low-Power Multimedia DSP Systems," ECE Dept. Colloq. talk at North Carolina State University, Nov. 30, 1998

75. "Low-Power DSP Components for Multimedia Communications," National Univ. of Singapore, Feb. 22, 1999

76. "Low-Power DSP Components for Multimedia Communications," University of California-Davis, March 10, 1999

77. "Low-Power DSP Components for Multimedia Communications," Broadcom Corporation, March 18, 1999

78. Lectures on VLSI Signal Processing, Lund University, April-May 1999

79. Lectures on VLSI Signal Processing, KTH Royal Institute of Technology, Stockholm, May 1999

80. "Low-Power and High-Speed Computer Arithmetic Architectures," Stanford University, Nov. 23, 1999

81. "Low-Power DSP Components for Multimedia Communications," IEEE Orange County section, Oct. 23, 2000

82. "Low-Power DSP Components for Multimedia Communications," U.C. Santa Barbara, April 20, 2001

83. "Low-Power DSP Components for Multimedia Communications," U.C.L.A., May 16, 2001

84. "Low-Power DSP Systems," NEC Corp., Japan, July 26, 2001

85. "Low-Power DSP Components for Multimedia Systems," Invited Talk at System-on-Chip Conference, Nov. 2001, Tampere

86. "VLSI Architectures for Digital Signal Processing Systems," Invited Talk at St. Cloud State, April 26, 2002

87. "Architectures for Broadband Communications Systems," Seoul National University, Seoul, Korea

88. "Design of High-Speed DSP Receivers," Lund University, Sweden, Sept. 2003

89. "Design of High-Speed DSP Receivers," Linkoping University, Sweden, Sept. 2003

90. "Architectures for Broadband Communications Systems," National Taiwan University, Taipei, Taiwan, Nov. 2003

91. "Architectures for Broadband Communications Systems," National Chiao-Tung University, Taiwan, Nov. 2003

92. "Architectures for Broadband Communications Systems," National Cheng-Kung University, Taiwan, Nov. 2003

93. "VLSI Architectures for Turbo and LDPC Codes," University of California, San Diego, August 2004

94. Presented a talk on "Data Fusion" on Dec. 20, 2006 at Medtronic, Inc.

95. Eminent Speakers Series Colloquim at the University of Virginia (Electrical Engineering Dept.) on Feb. 23, 2007

96. Presented a talk on "Electricity" to 4th Grade students at Providence Academy, April 2007

97. Series of 6 talks on Biomedical Signal Processing, Feature Extraction and Classification at Medtronic, April-May 2007

98. "Feature Extraction and Classification of Biomedical Signals," Indian Institute of Technology, Kharagpur, Jan. 3, 2008

99. "Feature Selection and Classification in Heart Sound," Tech Tuneup, UMN, June 2008

100. Talk on Seizure Prediction, UMN Neuroengineering Center, May 2009

101. Talk on EEG Signal Processing, Medtronic, June 2009

102. Talk on EEG Signal Processing, U.C. Berkeley, Aug. 2009

103. "Signal Processing Device for Seizure Prediction," Neuroengineering Symp., University of Minnesota, Feb. 2, 2010

104. "Digital Signal Processing with Protein Molecules and DNA Strands," Information Systems Lab (ISL) Colloquium, Stanford, Nov. 9, 2010

105. "Digital Signal Processing with Protein Molecules and DNA Strands", CHESS Seminar, University of California, Berkeley, Nov. 10, 2010

106. "Seizure Prediction and Detection", Neuroengineering Symposium, Univ. of Minnesota, Feb. 9, 2011

107. "Processing Signals from EEG Electrodes and Protein Molecules: Convergence of DSP, Machine Learning, and Digital Design," Broadcom, June 7, 2011

108. "Digital Signal Processing for Embedded Communications and Biomedical Systems at Samsung", Korea, May 23, 2012

109. "Language Understanding of Schizophrenic Patients from MEG Data," Neuroengineering Symposium, Univ. of Minnesota, Feb. 16, 2012

110. "Ethics and Professional Conduct for Electrical Engineers," North Central Electrical Engineering Society (NCEES), Minneapolis, October 15, 2013

111. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Distinguished Speaker Series, ECE Department, University of Arizona, April 24, 2014

112. "VLSI Computing of Digital Signal Processing Functions," University of Alberta, October 16, 2014

113. "Biomarkers and Brain Connectiviy for Neurological and Psychiatric Disorders", Electrical Engineering Distinguished Talk, University of Alberta, Oct. 17, 2014

114. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Minneapolis VA Center, Sept. 28, 2015

115. "Molecular Machine Learning Systems," Workshop on Coding Techniques for Synthetic Biology at the University of Illinois, Urbana, October 30, 2015

116. "Fundus Image Analysis for Retinopathy using Signal Processing and Machine Learning," Univ. of Calgary, Dec. 14, 2015

117. "Network Analysis of Human Brain Connectivity in Psychiatric Patients and Healthy Humans," Neuroengineering/Neuroimaging Seminar, UMN, Feb. 18, 2016

118. "Architectures for Emerging Industrial Internet of Things: Reducing Energy and Enhancing Security," Invited Talk at 2016 NTU-MediaTek IC Design Workshop, Nanyang Technological University, Singapore, Aug. 10, 2016

119. "Brain, Biomedical, and Biomolecular Informatics: Convergence of Signal Processing, Machine Learning and Computing," ECE Colloquium Talk at University of Washington, Seattle, Oct. 25, 2016

120. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," ECE Colloquium Talk at Cornell, Oct. 31, 2016

121. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," IEEE Student Branch, Indian Institute of Technology, Khaagpur, India, Dec. 26, 2016

122. "Computing Signal Processing and Machine Learning Functions using DNA," Indian Institute of Technology, Bhubaneswar, India, Jan. 4, 2017

123. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," S O A University, Bhubaneswar, India, Jan. 6, 2017

124. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Technology - Madras, Chennai, India, Jan. 9, 2017

125. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Science, Bengaluru, India, Jan. 10, 2017

126. "Authentication and Functional Obfuscation of Integrated Circuits," Texas Instruments, Bengaluru, India, Jan. 13, 2017

127. "Internet of Things: Energy-Efficient Machine Learning Classification and Hardware Security," University of Illinois at Chicago, April 21, 2017

128. "Authentication and Functional Obfuscation of Integrated Circuits," Shanghai Jiao Tong University, June 28, 2017

129. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Talk in Computer Science and Engineering Dept., Indian Institute Technology, New Delhi, Aug. 25, 2017

130. "Information Analytics, Energy-Efficiency and Hardware Security for Internet-of-Things Applications," Seoul National University, Jan. 26, 2018

131. "Data Analytics and Data-Driven Computing: Applications from Internet-of-Things to Classifying Neuropsychiatric Disorders," University of Texas at Austin, Feb. 15, 2018

132. "Multi-Dimensional Time-Series Data Analysis: A Convergence of Signal Processing and Machine Learning," Shanghai Maritime University, June 8, 2018

133. "Design of Features and Classifiers for Neuro-Psychiatric Disorders via Machine Learning," Fudan University, School of Microelectronics, June 19, 2018

134. "VLSI Architectures for Low-Energy Machine Learning Systems," Fudan University, School of Microelectronics, June 20, 2018

135. "Authentication and Obfuscation of Integrated Circuits," Fudan University, School of Microelectronics, June 21, 2018

136. "VLSI Architectures for Low-Energy Machine Learning Systems," Xi'an Jiao Tong University, School of Microelectronics, July 1, 2018

137. "Internet of Things: Energy-Efficient Data Analytics, and Hardware Security," Tsinghua University, School of Microelectronics, Beijing, China, July 24, 2018

138. "Seizure Prediction and Detection using Machine Learning," Nanyang Technological University (NTU), Singapore, August 30, 2018

139. "Brain Disorders, Brain Connectivity Analysis and Brain-Inspired Computing," Nanyang Technological University (NTU), Singapore, August 31, 2018

140. "Machine Learning: Low-Energy Architectures and Applications," Indian Institute of Technology, Kharagpur, India, September 5, 2018

141. "Machine Learning: Low-Energy Architectures and Applications," Indian Institute of Technology, Bhubaneswar, India, September 6, 2018

142. "Low-Energy VLSI Architectures for Machine Learning Systems and Applications," Stanford University, Oct. 8, 2018

143. "Low-Energy VLSI Architectures for Machine Learning Systems and Applications," Intel, Santa Clara, Oct. 10, 2018

144. "Machine Learning Systems: Low-energy VLSI Architectures and Applications," University of California-Irvine, November 16, 2018

145. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," Universidad Nacional de Cordoba, May 3, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

146. "Authentication and Obfuscation of Integrated Circuits," Universidad Tecnologica Nacional, May 8, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

147. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," Universiti Putra Malaysia, Selangor, Malaysia, June 28, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

148. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," Universiti Teknologi PETRONAS, Perak, Malaysia, July 1, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

149. "Authentication and Obfuscation of Integrated Circuits," Technical University Gh. Asachi of Iasi, Romania, July 19, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

150. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," Technical University Gh. Asachi of Iasi, Romania, July 22, 2019 [IEEE Circuits and Systems Society Distinguished Lecture]

151. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," University of Saskatchewan, Saskatoon, Canada, September 27, 2019

152. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," Texas A&M University Distinguished Lecture, November 1, 2019

153. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," Google, November 6, 2019

154. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," IEEE CASS-SH Artificial Intelligence For Industry (AI4I) Forum- Fall 2019, Shanghai, China, Nov. 24, 2019

155. "Brain Inspired Computing: Low-Energy Neuromorphic Computing Accelerator Architectures," IEEE CASS Seasonal School on AI-Driven Circuit, System and EDA Tools, Shanghai, China, Nov. 26, 2019

156. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," National Technical University of Athens, March 6, 2020

157. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," Aristotle University of Thessaloniki, March 9, 2020

158. "Obfuscation and Authentication of Integrated Circuits," Aristotle University of Thessaloniki, March 10, 2020

159. "Machine Learning and Deep Learning Systems: Low-Energy VLSI Architectures and Applications," IEEE Circuits and Systems Society Virtual Distinguished Lecture Webinar, April 29, 2020

160. "Hardware Security: Functional Encryption and Chip Authentication," IEEE CASS Rio Grande do Sul Chapter Virtual Distinguished Lecture, September 4, 2020

161. "Introduction to VLSI DSP Systems," Indian Institute of Technology, Bhubaneswar, India, Feb. 26, 2021 (Indo-USA Short-Term Course on "VLSI Architectures for Energy-Efficient Embedded Healthcare Systems")

162. "VLSI DSP Architectures: Fast Convolution, FIR and IIR Digital Filters and Fast Fourier Trasnforms," Indian Institute of Technology, Bhubaneswar, India, Feb. 27, 2021 (Indo-USA Short-Term Course on "VLSI Architectures for Energy-Efficient Embedded Healthcare Systems")

163. "Machine Learning Architectures: Neural Networks, Multilayer Perceptron, Restricted Boltzmann Machine, Deep Convolutional Neural Networks," Indian Institute of Technology, Bhubaneswar, India, Feb. 28, 2021 (Indo-USA Short-Term Course on "VLSI Architectures for Energy-Efficient Embedded Healthcare Systems")

164. "Data Analytics and Data-Driven Computing: Applications from IoT to Classifying Disorders," Indian Institute of Technology, Bhubaneswar, India, March 26, 2021 (Indo-USA Short-Term Course on "Signal Processing and Machine Learning Techniques for Data-Driven IoT and Smartphone Health Monitoring")

165. "Brain Inspired Computing: Development of the Perceptron and Multi-Layer Perceptron followed by CNNs and RNNs" Indian Institute of Technology, Bhubaneswar, India, March 27, 2021 (Indo-USA Short-Term Course on "Signal Processing and Machine Learning Techniques for Data-Driven IoT and Smartphone Health Monitoring")

166. "Minimum Uncertainty and Sample Elimination based Binary Feature Selection and Incremental-Precision based Feature Computation and Multi-Level Classification for Low-Energy IoT," Indian Institute of Technology, Bhubaneswar, India, March 30, 2021 (Indo-USA Short-Term Course on "Signal Processing and Machine Learning Techniques for Data-Driven IoT and Smartphone Health Monitoring")

167. "Teaching Digital Signal Processing by Partial Flipping, Active Learning, and Visualization: Keeping Students Engaged," IEEE Twin Cities SP/COM Chapter, July 22, 2021 [IEEE SPS Distinguished Lecture]

168. "Machine Learning Systems: Low-Energy VLSI Architectures and Applications," IEEE Circuits and Systems Society Hyderabad Chapter, Oct. 8, 2021 [IEEE CASS Distinguished Lecture]

169. "Accelerator Architectures for Deep Neural Networks: Inference and Training," University of Minnesota, Dept. Electrical & Computer Engineering, Colloquium Talk, November 4, 2021

170. "Accelerator Architectures for Deep Neural Networks: Inference and Training", University of Lisbon, November 19, 2021 [IEEE CASS Distinguished Lecture]

171. "Accelerator Architectures for Deep Neural Networks: Inference and Training," EPFL, Lausanne, November 29, 2021 [IEEE CASS Distinguished Lecture]

172. "Accelerator Architectures for Deep Neural Networks: Inference and Training," ETH, Zurich, December 1, 2021 [IEEE CASS Distinguished Lecture]

173. "Accelerator Architectures for Training Deep Neural Networks," IEEE CASS Santa Clara Valley Chapter, January 20, 2022 [IEEE CASS Distinguished Lecture]

174. "Hardware Security: Functional Encryption and Homomorphic Encryption Acceleration, International Conference on Emerging Trends and Technologies on Intelligent Systems (ETTIS), March 22, 2022 [Keynote Talk]

175. "Hardware Security: Functional Encryption and Chip Authentication," MEST Center Webinar, University of Florida, Gainesville, April 20, 2022

176. "Accelerator Architectures for Deep Neural Networks: Inference and Training," Booz, Allen, Hamilton Colloquium at the University of Maryland, May 6, 2022

177. "Brain-Inspired Computing: Models and Architectures, Indian Institute of Technology, Bhubaneswar, India, Nov. 1, 2022

178. "Hyperdimensional Computing, Indian Institute of Technology, Bhubaneswar, India, Nov. 10, 2022

179. "Brain Network Analysis: Classification of Mental Disorders, Indian Institute of Technology, Bhubaneswar, India, Nov. 15, 2022

180. "Architectures for Post-Quantum Cryptography and Homomorphic Encryption: Towards a Quantum-Safe Society, Indian Institute of Technology, Bhubaneswar, India, Nov. 22, 2022

181. "VLSI Architectures for Training Deep Neural Networks and for Homomorphic Encryption, Indian Institute of Technology, Kanpur, India, Dec. 1, 2022 [Computer Science Department Talk]

182. "Accelerator Architectures for Deep Neural Networks: Inference and Training, 2022 International Conference on Recent Trends in Microelectronics, Automation, Computing and Communication Systems (ICMACC), Hyderabad, Dec. 28, 2022 (Remote) [Keynote Talk]

183. "Hardware Security: Functional Encryption and Chip Authentication, IEEE Rock River Valley Lecture, Jan. 26, 2023 (Remote)

184. "The Era of Pervasive General Intelligence," Emerging Trends and Technologies on Intelligent Systems (ETTIS-2023), Feb. 23, 2023 (Remote) [Keynote Talk]

185. "VLSI Architectures for Training Deep Neural Networks and for Homomorphic Encryption," University of Virginia, Colloquium Talk in the Electrical & Computer Engineering Department, April 14, 2023

186. "Accelerator Architectures for Deep Neural Networks: Inference and Training," Marvell Argentina, Cordoba, August 23, 2023

187. "VLSI Accelerators Architectures for Training Deep Neural Networks," Fudan University, Shanghai, December 10, 2023

188. "VLSI Accelerators Architectures for Training Deep Neural Networks," IEEE Solid State circuits Shanghai Chpater, Wuxi, December 14, 2023

189. "Accelerator Architectures for Post Quantum Cryptography and Homomorphic Encryption," 5th International Symposium on Smart and Healthy Cities, Hainan, China, December 16, 2023 [Keynote Talk]

190. "Accelerator Architectures for Post Quantum Cryptography and Homomorphic Encryption," Fudan University, Shanghai, December 18, 2023