Reliable Power Delivery for 3D ICs

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Power Supply Integrity in 3D

- Putting the power in is as important as getting the heat out
- Higher current density, faster current transients worsen supply noise
- Greater challenge in 3D due to via resistance, limited number of supply pins

Current per pin (2D) – ITRS

![Diagram of 2D and 3D power delivery systems]
Thermal challenges

- Each layer generates heat
- Heat sink at the end(s)

- Simple analysis
  - $\frac{\text{Power}(3D)}{\text{Power}(2D)} = m$
  - $m = \# \text{ layers}$
  - Let $R_{\text{sink}} =$ thermal resistance of heat sink
  - $T = \text{Power} \times R_{\text{sink}}$
  - $m$ times worse for 3D!

- And this does not account for
  - Increased effective $R_{\text{sink}}$
  - Leakage power effects, T-leakage feedback

- Thermal bottleneck: a major problem for 3D

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Power delivery challenges

- Each layer draws current from the power grid
- Power pins at the extreme end tier(s)

- Simple analysis
  - $\frac{\text{Current}(3D)}{\text{Current}(2D)} = m$
  - $m = \# \text{ layers}$
  - Let $R_{\text{grid}} =$ resistance of power grid
  - $V_{\text{drop}} = \text{Current} \times R_{\text{grid}}$
  - $m$ times worse for 3D!

- And this does not account for
  - Increased effective $R_{\text{grid}}$
  - Leakage power effects, increased current due to T-leakage feedback

- Power bottleneck: a major problem for 3D
Power Supply Integrity Characteristics

**2D versus 3D**
- Low frequency noise: 3D > 2D
- Mid frequency noise: 3D \( \approx \) 2D
- High frequency noise: 3D \( \approx \) 2D
- Resonant frequency: 2D > 3D

**Tier versus tier**
- Low/mid frequency noise: \( Z_1 > Z_2 > Z_3 \)
- High frequency noise: \( Z_3 > Z_1 > Z_2 \)
- Resonant frequency: \( Z_1 \approx Z_2 \approx Z_3 \)

Packaging technologies

- Wire bonding
- Stacked package/stacked die
- Flip-chip
- 3D integration
Traditional power delivery

- Requirements
  - $V_{dd}$, GND signals should be at correct levels (low V drop)
  - Electromigration constraints
    - Current density must never exceed a specification
    - For each wire, $I/w < J_{spec}$
  - $dI/dt$ constraints
    - Need to manage $dI/dt$ to reduce inductive effects

- Techniques for meeting constraints
  - Widening wires
  - Using appropriate topologies
  - Adding decoupling capacitances

- Already challenged for 2D technologies
  - Reliable power delivery hard
  - Decaps get leaky
- Circuit + CAD approaches necessary

Outline of the talk

- Motivation
- Switched decaps
- Multistory Vdd
- CMOS+MIM decaps
Active supply noise cancellation

- Charge provided by switched decap (=0.5C·Vdd+CΔVdd/2) much larger than that of a conv. decap (=2C·ΔVdd)
- For a supply noise (ΔVdd) of 5%, effective decap value is boosted by 7.5X

Supply noise cancellation: Results

- 200pF switched decap has lower noise than 1200pF conventional decap
- 5−11X boost over passive decaps depending on supply noise magnitude
Proof of concept: Switched decap test chip

- Technology: 0.13µm CMOS
- Quiescent Current: 0.54mA
- Regulation Freq. (w/o decap): 10MHz-300MHz
- Regulator Area (w/o decap): 100µmx70µm
- Regulator Area (w/ 300pF decap): 190µmx220µm
- Total Die Area: 0.9mmx1.8mm

- 2.2-9.8dB reduction of the 40MHz resonant noise using 100-300pF switched decaps

Comparison with passive damping

<table>
<thead>
<tr>
<th>Swdecap Value</th>
<th>Resonant Suppression</th>
<th>Equivalent Passive Decap</th>
<th>Decap Boost</th>
</tr>
</thead>
<tbody>
<tr>
<td>100pF</td>
<td>2.2dB</td>
<td>500pF</td>
<td>5X</td>
</tr>
<tr>
<td>200pF</td>
<td>5.5dB</td>
<td>1500pF</td>
<td>7.5X</td>
</tr>
<tr>
<td>300pF</td>
<td>9.8dB</td>
<td>3500pF</td>
<td>11X</td>
</tr>
</tbody>
</table>
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Multi-story power supply

<table>
<thead>
<tr>
<th></th>
<th>1-story</th>
<th>2-story</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>2I</td>
<td>I</td>
</tr>
<tr>
<td>Voltage</td>
<td>Vdd</td>
<td>2Vdd</td>
</tr>
<tr>
<td>Power</td>
<td>2Vdd·I</td>
<td>2Vdd·I−Δ</td>
</tr>
<tr>
<td>Noise</td>
<td>15%Vdd</td>
<td>&lt; 8%Vdd</td>
</tr>
</tbody>
</table>

Improved supply noise due to:
- Reduced current magnitude
- Cleaner middle supply voltage

Attractive for 3D chips:
- Isolated substrate for each tier
- Chip is naturally partitioned
Multi-story power supply: Test layout

- A test layout in MITLL’s SOI process shows a 5.3% area overhead

CAD solutions for multi-story circuits
Overall Design Flow

- Netlist and block information
- Floorplanning involving regular modules and regulators
- Assigning modules using a graph partition-based algorithm
- Module assignment

Estimating the wasted power

\[ G_{\text{VVM}} = V_{\text{VM}} \times d_{\text{di}} \]

\[ \sum_{i=1}^{n} x_{ji} \leq x_{ij} \sum_{i=1}^{n} t_{ji} x_{ii} - t_{ji} x_{ij} \]

\[ \sum_{i=1}^{n} x_{ji} \leq x_{ij} \sum_{i=1}^{n} t_{ji} x_{ii} - t_{ji} x_{ij} \]

\[ x_i = 0 \quad \text{if} \quad x_i = x_j \]

\[ x_i = 1 \quad \text{if} \quad x_i \neq x_j \]

Graph partitioning problem!
Constructing the graph

3D benchmarks

- Exercised on GSRC floorplanning benchmarks
- Largest floorplan has 300 modules
- Comparison with (slow)simulated annealing method

<table>
<thead>
<tr>
<th>Layer</th>
<th>Wasted Power (%)</th>
<th>Maximum IR Noise (mV)</th>
<th>Runtime (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Partition-Based</td>
<td>Annealing</td>
<td>Partition-Based</td>
</tr>
<tr>
<td>n100Layer0</td>
<td>3.3</td>
<td>52.8</td>
<td>0.03</td>
</tr>
<tr>
<td>n100Layer1</td>
<td>3.1</td>
<td>28.9</td>
<td>0.02</td>
</tr>
<tr>
<td>n100Layer2</td>
<td>3.7</td>
<td>45.4</td>
<td>0.02</td>
</tr>
<tr>
<td>n200Layer0</td>
<td>8.7</td>
<td>55.2</td>
<td>0.31</td>
</tr>
<tr>
<td>n200Layer1</td>
<td>5.6</td>
<td>62.1</td>
<td>0.16</td>
</tr>
<tr>
<td>n300Layer0</td>
<td>5.6</td>
<td>55.7</td>
<td>0.18</td>
</tr>
<tr>
<td>n300Layer1</td>
<td>6.3</td>
<td>61.1</td>
<td>1.83</td>
</tr>
<tr>
<td>n300Layer2</td>
<td>5.4</td>
<td>61.1</td>
<td>0.69</td>
</tr>
</tbody>
</table>

Runtime Comparison: > $10^3$ x speedup over SA
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• Motivation
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MIM decaps

• Capacitance density*
  – CMOS – 17.3 fF/μm² at 90nm
  – MIM – 8.0 fF/μm²
• Leakage density*
  – CMOS – 1.45e-4 A/ cm²
  – MIM – 3.2e-8 A/cm²
• Congestion
  – MIM – routing blockage

* Numbers deduced from Roberts et al., IEDM05 and PTM simulations
Overall flow of the algorithm

1. **3D layout info.**
2. **Technology parameters**
3. Build 3D power grid
4. Transient power grid analysis
5. **Noise metric \( S \neq 0 \)?**
   - **Yes:** Linear programming based decap allocation
   - **No:** Stop

Metrics

- **Noise:** Optimize the integral of noise violation over time
  
  - **Waveform of node \( j \) on VDD grid**
  
  - **Z:**
    \[
    z(\lambda) = \sum z(\lambda)
    \]

- **Linearized congestion metric**
  
  \[
  \Delta Cong_k = \sum_{i \in R_k} (\lambda_i \cdot \Delta y_i)
  \]

  - \( R_k \) is the set of grid cells adjacent to grid \( k \)
  - \( \lambda \) reflects the effect on the congestion of grid \( k \) after inserting a small MIM decap \( \Delta y \) in grid \( i \).
Sequence of linear programs: formulation

- Objective
  \[
  \min \alpha \Delta S + (1-\alpha) \Delta P
  \]
  \[
  \Delta S = \sum_k (a_k \Delta x_k + b_k \Delta y_k) = \text{change of violation area}
  \]
  \[
  \Delta P = \sum_k (c_k \Delta x_k + d_k \Delta y_k) = \text{change in leakage}
  \]
  \[
  \Delta x_k: \text{Newly added CMOS decap to grid } k
  \]
  \[
  \Delta y_k: \text{Newly added MIM decap to grid } k
  \]
- Constraints
  - Congestion constraint
    \[
    \Delta \text{Cong}_k \leq \gamma \cdot \text{Cong}_k
    \]
  - Decap resource constraint
    \[
    0 \leq \Delta x_k \leq \min\{\Delta_{CMOS}^k, C_{CMOS}^k\}
    \]
    \[
    0 \leq \Delta y_k \leq \min\{\Delta_{MIM}^k, C_{MIM}^k\}
    \]

Experimental results

<table>
<thead>
<tr>
<th>Ckt</th>
<th># Nodes</th>
<th>Worst V droop (V)</th>
<th># nodes with noise violations</th>
<th>Violation Area S (V ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ibm123</td>
<td>18,634</td>
<td>0.135</td>
<td>3330</td>
<td>13.739</td>
</tr>
<tr>
<td>ibm05</td>
<td>12,026</td>
<td>0.122</td>
<td>1359</td>
<td>72.260</td>
</tr>
<tr>
<td>ibm08</td>
<td>17,030</td>
<td>0.125</td>
<td>3191</td>
<td>41.305</td>
</tr>
<tr>
<td>ibm10</td>
<td>29,262</td>
<td>0.159</td>
<td>5935</td>
<td>91.286</td>
</tr>
<tr>
<td>ibm18</td>
<td>75,042</td>
<td>0.163</td>
<td>6392</td>
<td>108.649</td>
</tr>
</tbody>
</table>
Conclusion

• Power delivery into a 3D chip is a critical problem for next-generation designs

• Incremental solutions will only take us so far
  – Already stretched even for 2D designs

• Need innovative design + CAD solutions